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Power Electronic Systems Laboratory

Power Electronic Systems Laboratory
Prof. Dr. Johann W. Kolar Autumn Semester 2015

Semester Thesis

Energy Storage For Mechatronic Energy Harvesting System

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Supervisor: Michael Flankl

Acknowledgments

My special thanks go to Professor Dr. Johann Walter Kolar who gave me the chance to work on the specific project concerning the energy storing. The completion of the thesis could not have been possible without the assistance of my supervisor Michael Flankl whose contributions are sincerely appreciated and gratefully acknowledged.

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Nikolaos Chrysogelos

Energy Storage for Mechatronic Energy Harvesting System
CONFIDENTIAL

A. Description

With the ongoing trend of integration in mechatronics, energy harvesting systems are gaining in importance. In these systems, power is harvested by a transducer and delivered to the load, e.g. an actuator. In order to cover the power demand of a pulsed load, the integration of an energy storage system is highly beneficial as it allows dimensioning the harvesting transducer for the average load power, resulting in reduced size of the system.

For an ongoing energy harvesting research project at PES, carried out in cooperation with a world leading mechatronic systems manufacturer, an energy storage system with series connected super capacitors and power electronics interface to a DC bus supplying the load converter is under consideration.

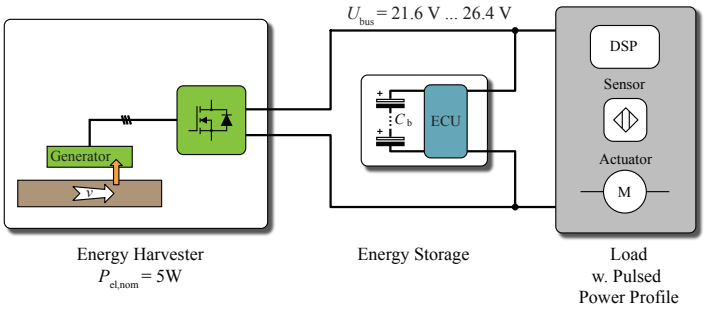


Figure 1: Schematic overview of energy storage system.

B. Project Task

This Semester Thesis focuses on the energy storage according to **Fig. 1**. Firstly, the system structure and the control scheme of said energy storage are analyzed, simulated and optimized for the power profiles given in **Fig. 2**. Secondly, an energy storage demonstrator is implemented based on an already existing DC/DC converter and measurements are conducted. Depending on the progress of the work, a load system implementing the load power profile (cf. **Fig. 2**) is set up and a mutual test of energy storage and load system concludes the work.

Tasks

- Analysis and optimization of storage topology
- Analysis and simulation of control scheme
- Hardware implementation of energy storage
- Software implementation of the selected control scheme
- Test of energy storage demonstrator

- Implementation of load system (progress depending)
- Mutual test of load and energy storage (progress depending)
- Documentation of work
- Final presentation

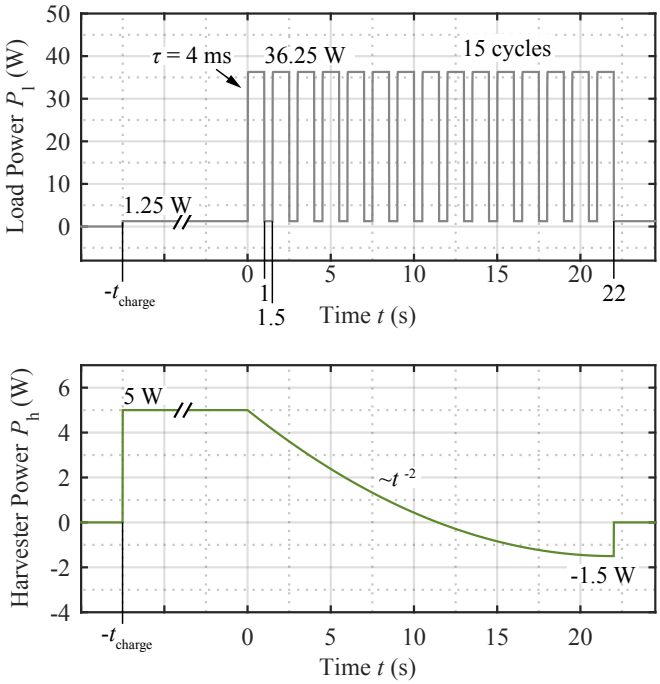


Figure 2: Power profile of harvester and load.

C. Documentation and Project Presentation

All scientifically relevant results must be documented. This includes a detailed description of the procedure, calculations, simulations, measurements, and results. A presentation summarizing the project will be given once the project is completed.

D. General Information

The document entitled *Vorschriften über die Durchführung von internen Studien- und Masterarbeiten* (yellow sheet) constitutes the integral parts of this project. The document entitled *Sicherheitsvorschriften* (red sheet) must be strictly followed. The white form entitled *Gefahrenabschätzung am Arbeitsplatz und Handhabung der Software auf Rechnern der Professur* will be filled out and handed to Peter Albrecht in room ETL H11. The *Abgabekarte* must be kept until the end of the project.

Period:	Project Start:	Monday, 5.10.2015
	Final Presentation:	January 2016, t.b.d
	Project Deadline:	Thursday, 31.12.2015
Supervisor:	Michael Flankl, ETL H 17, E-Mail: flankl@lem.ee.ethz.ch	

Contents

Abstract

The aim of this thesis was the design of an efficient passive storage unit which would be able to absorb energy from a harvester sensor and deliver it to a load according to its power profile. Furthermore, a control system was implemented such that a bus voltage of 24V $\pm 10\%$ will be kept constant and stable. Firstly, the system structure and operation were explained and optimized while the selection of the components was analyzed. Secondly, the control scheme was presented and the circuit along with the control algorithm was implemented in GeckoCircuits to verify its functionality. Finally, one charging cycle was performed to evaluate the system performance and efficiency.

Nomenclature

Symbols

A	Area	in m^2
A_L	Inductance factor	in $\frac{\mathrm{H}}{\mathrm{turn}}$
A_c	Effective Magnetic Area	in mm^2
B	Magnetic flux density	in T
B_{pk}	Peak magnetic flux density	in T
C	Capacitance	in F
d_o	Outer Diameter	in mm
d_i	Inner Diameter	in mm
E	Energy	in J
ESR	Parasitic resistance of the Capacitor	in Ω
f	Frequency	in Hz
H	Magnetic field	in $\mathrm{A} \cdot \mathrm{m}^{-1}$
I	Current	in A
I_{RMS}	RMS Current	in A
J	Current density	in $\frac{\mathrm{A}}{\mathrm{mm}^2}$
k_{lin}	Winding fill factor	
K_p	Proportional Term	
K_i	Integral Term	
K_u	Winding fill factor	
L	Inductance	in H
l_g	Air gap length	in mm
l_e	Effective Magnetic length	in mm
η	efficiency	in %
$\overline{P}$	Average Power	in W
P_V	Power losses per Volume	in W
p	Instantaneous power	in W
$price$	Price	in CHF
R	Resistance	in Ω

ρ_{cu}	Wire resistivity	in $\Omega \cdot$ cm
t	Time / duration	in s
T	Temperature	in K
T	Period	in s
Θ	Temperature	in ^{o}C
V	Voltage	in V
V_e	Volume	in l, (dm^3)

Acronyms and Abbreviations

ADC	Analog-to-Digital Converter
DSP	Digital Signal Processor
ESU	Energy Storage Unit
ETH	Eidgenössische Technische Hochschule
ELCO	Electrolytic Capacitors
ISR	Interrupt Service Routine
PCB	Printed Circuit Board
PES	Power Electronic Systems (Laboratory)
PWM	Pulse-Width Modulation
SC	Super Capacitor
TFB	Thin Film Battery

Chapter 1

Introduction

Due to the ongoing trend of mechatronics integration, energy harvesting systems have attracted the interest of industry and research development. They are consisted of an energy harvester capable of capturing power from an external source and deliver it to a load. The use of an energy management circuit connected between the harvester and the load may be highly beneficial as it provides an efficient way of energy storage, voltage stability across the bus of the system and allows power delivery according to the needs of the load. As a result, the Energy Storage Unit (ESU) may contribute in reducing the overall size of the harvester and the system. The scope of this chapter is the investigation of the structure of the ESU as well as the appropriate dimensioning of the components of the unit.

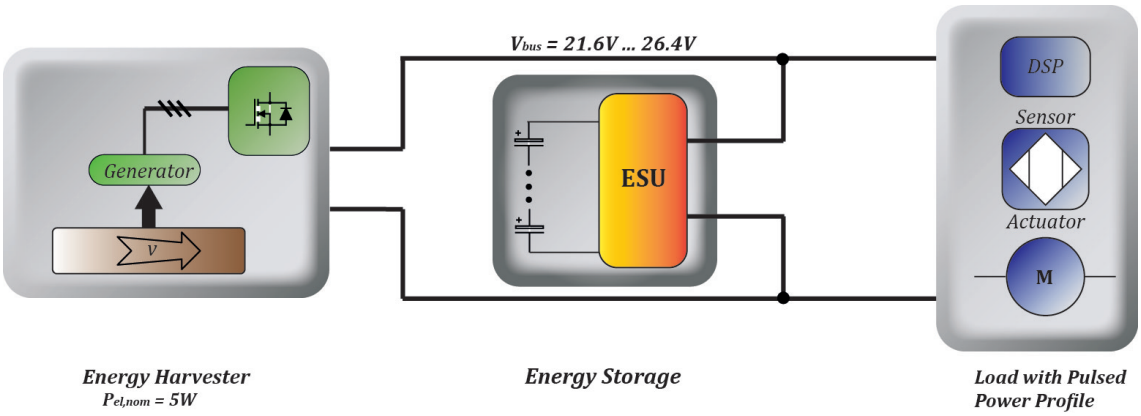


Figure 1.1: Full schematic Overview of Energy Harvesting System.

1.1 Overview

For the underlying project the goal is to complete a power supply system using relative motion of a conductive surface. The energy harvester provides power to the bus which is stored in the ESU

and when it is fully charged it is delivered to a pulsed load. The schematic overview of the energy storage system under consideration is in Fig. 1.1.

The energy harvester of the above system is a contactless electromechanical device which absorbs energy from the interaction with a rotating wheel. The nominal Power is considered $P_{\text{el}} = 5\text{W}$ while it exhibits the Power Profile described in Fig. 1.2.

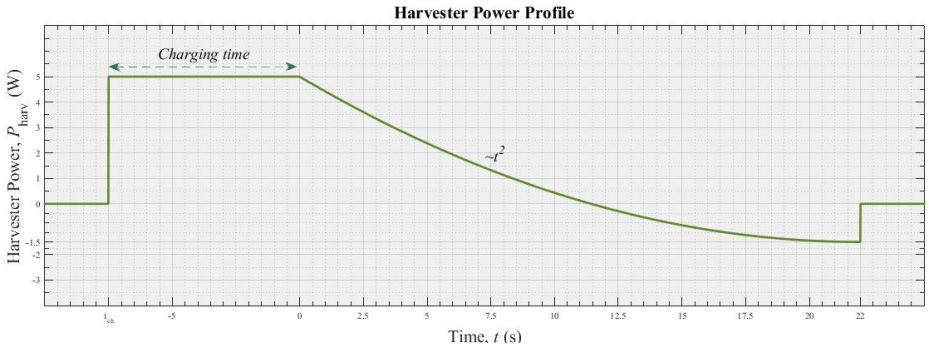


Figure 1.2: Power profile of Energy harvester.

$$P_{harv} = \begin{cases} 5 \text{ W}, & -t_{charge} \leq t \leq 0 \\ 6.5 \cdot \left(1 - \frac{t}{22}\right)^2 - 1.5, & 0 \leq t \leq 22 \end{cases}$$

The load in our system can be simulated by a varying power resistor and its power profile is given on the Fig. 1.3.

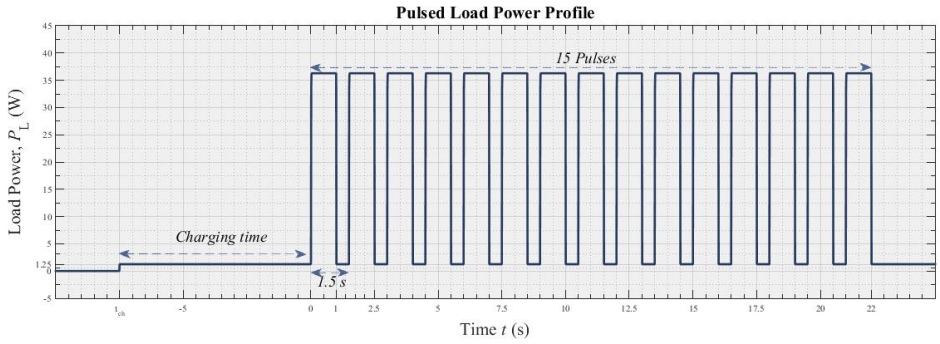


Figure 1.3: Power profile of the actuator.

$$P_L = \begin{cases} 1.25 \text{ W}, & -t_{charge} \leq t \leq 0 \\ 35 \cdot rect(t) + 1.25, & 0 \leq t \leq 22 \end{cases}$$

where

$$rect\,(t) = \begin{cases} 1 & 0 \leq mod(\frac{t}{1.5}) \leq 1 \\ 0 & 1 < mod(\frac{t}{1.5}) \leq 1.5 \end{cases} \qquad 0 \leq t \leq 22$$

Based on these two figures, it is asked to design and optimize the Energy Storage Unit so that it will be able to get charged by the Power profile of the generator in Fig. 1.2 at the beginning of each cycle (charging time, t_{ch}) and supply the corresponding power to the Load according to Fig. 1.3 (for 22 seconds). It is noted that the charging time during the start-up of the system will be different and larger than the charging time that is asked during each breaking cycle after the discharge of 22 seconds. For optimum design and minimization of the storage system, its power profile is excluded

$$P_{store} + P_{harv} = P_L \Longrightarrow P_{store} = P_L - P_{harv}$$

$$P_{store} = \begin{cases} -3.75 \text{ W}, & -t_{charge} \leq t \leq 0 \quad (charging\ time) \\ 35 \cdot rect\,(t) - 6.5 \cdot \left(1 - \frac{t}{22}\right)^2 + 2.75, & 0 \leq t \leq 22 \end{cases}$$

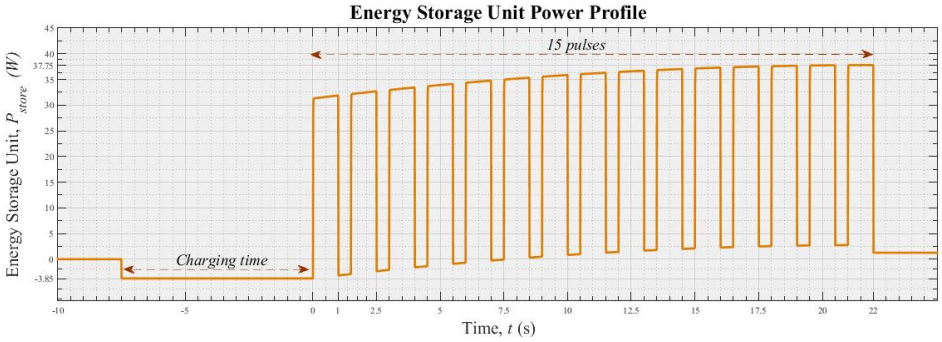


Figure 1.4: Power profile of the Energy Storage Unit.

1.2 Topologies of the Energy Storage System

In this section two different topologies of the energy harvesting system are considered in order to discuss the characteristics and the demands of the designed circuit.

1.2.1 Series Topology

The ESU is connected in series with the Harvesting system so that these two systems combined will give a bus voltage of 24V (Fig. 1.5). With this topology we may minimize the transistors of the converter since the voltage stress will be smaller. However, as the demands for the energy storage system remain the same, there is no significant difference in the volume of the storage unit.

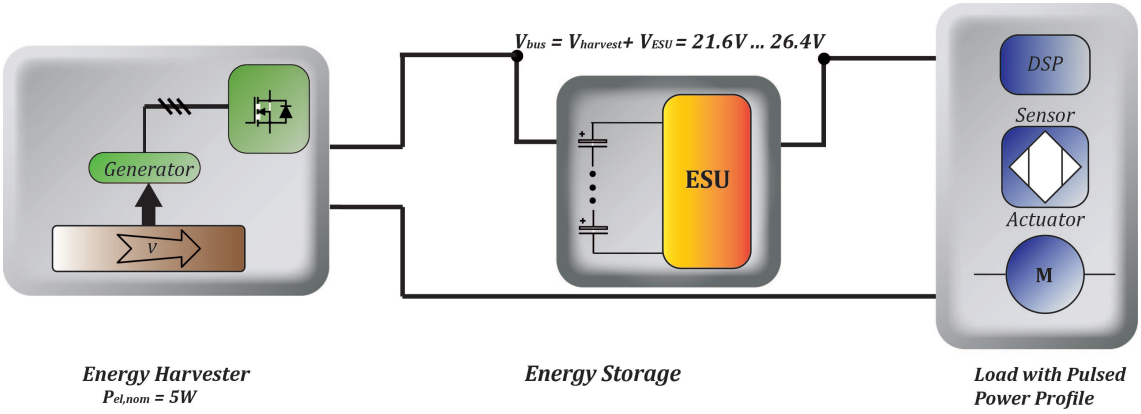


Figure 1.5: Energy Storage Unit in series with the load.

Moreover, this structure increases the complexity both on the hardware and the control software and it requires the harvester unit to provide the overall current to the load resulting in a larger transducer.

1.2.2 Parallel Topology

This is the most used topology (Fig. 1.1) in similar systems as it exploits at most the capabilities of the components of ESU as well as of the Energy harvester. In the next sections this topology is considered and analyzed.

1.3 Component design

The scope of this section is the optimization of the storage structure taking into consideration the volume, the cost and the charging/discharging efficiency of the system.

1.3.1 DC-DC conveter

On this section the use of the boost (Fig.1.6(a)) against the buck converter (Fig. 1.6(b)) during the discharge cycle is justified. To begin with, during the charging cycle the boost circuit would require transistors with higher voltage rating since the storing voltage would be higher than 24V ($V_{store} \geq 24$V) and therefore the stress on them would be higher. Thus the cost and the size would be significant larger. Moreover, the energy storage in higher than 24V would mean either the use of a lot of Supercapacitors in series since each piece usually have $V_{\text{nom}} \approx 3$V or electrolytic capacitors (ELCO) with $V_{\text{nom}} > 25$V which show serious disadvantages in the energy density figure in terms of cost and volume.

(a) Boost converter

(b) Buck conveter

Figure 1.6: Two types of conveter during the discharging cycle

1.3.2 Ceralink Capacitors

One growing technology of capacitor technology is produced by EPCOS CERALINK^{TM} which has very low ESR and ESL values, high current density and extremely low leakage currents. However, they are not suitable for our application since they exhibit low energy density which means it would be necessary to connect multiple capacitors ($\sim 3 \cdot 10^6$) in parallel to increase the capacitance of the system. They are mainly used for the reduction of the ripple of the output voltage as DC link capacitors. Commercial products are shown below.

Table 1.1: Comparison of Supercapacitors and Ceralink Capacitors.

Manufacturer	Price (CHF)	Cap.(F)	V_{nom} (V)	R_{ESR} (mΩ)	Volume (l)
Eaton Bussmann (SC)	6.84	$35F$	2.7V	20 mΩ	$6 \cdot 10^{-3}$
EPCOS (TDK)	16.00	$1\mu F$	500V	12 mΩ	$3.8 \cdot 10^{-4}$

Due to their high voltage capability, they would be suitable for boost circuits during the charging cycle. However, the low energy density per Volume which result in high volumes make them inappropriate for the corresponding application.

1.3.3 Supercapacitors and ELCO

Although an Aluminium capacitor may offer lower conduction losses due to low esr values and thus better efficiency, it is much bigger (155,667%), exhibits lower energy density (0.350 kJ/liter) and is 90% more expensive (268 CHF) than the first schematic which exploits only supercapacitors (21.2 kJ/liter, 0.006 liter, 6.48 CHF). In the case of a cheaper Aluminum Capacitor the efficiency might be extremely low due to high ESR losses. Thus, the use of such type of capacitor for energy storage cannot be in our choices.

Since the key parameters that are taken into consideration are efficiency ($\eta\%$), $volume(l)$ and $cost(CHF)$, it is evident that they don't meet the majority of them. Consequently the boost structure during the discharging stage along with supercapacitors will be discussed in the next sections.

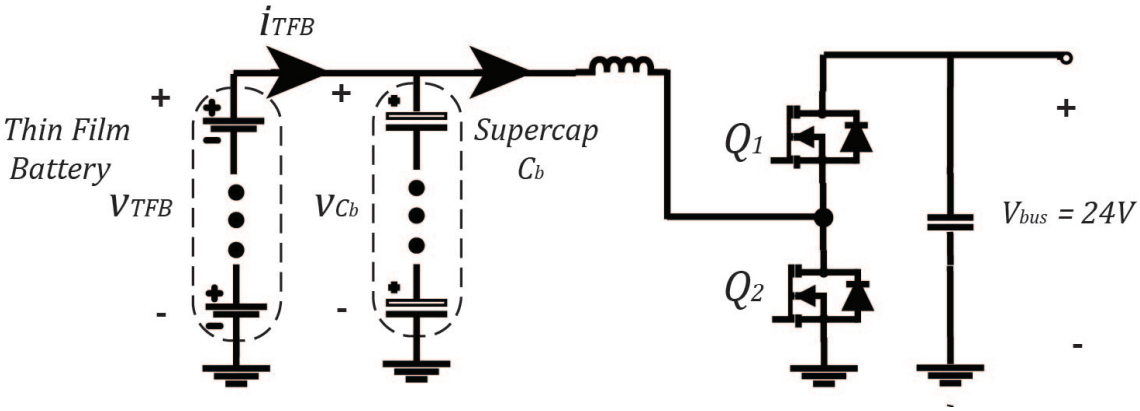


Figure 1.7: DC-DC converter with both Thin Film Battery and Supercapacitors.

Table 1.2: Comparison of Supercapacitors and ELCO.

Manufacturer	Price (CHF)	C (F)	V_{nom} (V)	R_{Esr} (mΩ)	Volume (l)
Eaton Bussmann (SC)	6.84 CHF	35 F	2.7 V	20 mΩ	0.006 l
Nichicon (ELCO)	268 CHF	2.2 F	10 V	5 mΩ	2 l
Vishay (ELCO)	192.5 CHF	1 F	25 V	5 mΩ	1.4 l
Nichicon (ELCO)	222.6 CHF	1 F	25 V	5 mΩ	2 l
Cornell CDE (ELCO)	226.5 CHF	1 F	20 V	5 mΩ	0.95 l

1.3.4 Supercapacitors and Thin Film Batteries

One of the most well-known elements in literature for Energy storage Units are Thin-Film Batteries and Supercapacitors. In this section these systems are discussed and their main characteristics are concluded.

In general, this structure is used widely both in energy harvesting applications and electric vehicles as the Thin Film Batteries exhibit great volumetric energy density and low cost per energy stored. Therefore, they are suited for applications with long energy supplies. However, in our scheme the cycle lasts only 22 seconds which can easily be handled by supercapacitors alone. Moreover the base load is 1.25 W and can be covered both from the harvester and the supercapacitors. The use of TFB would increase both the charging and discharging time (t_{ch}) which are not desirable on this application. Since the important factor of the system is the high power density, the TFB are redundant into our circuit. Another disadvantage is the addition of complexity and cost in the system as the parallel/series connection of Supercapacitors and TFB isn't that simple. A hybrid storage system needs a control system which manages the energy flow from both devices. As can be seen in the following table batteries also exhibit very high internal resistances resulting in reduced efficiency. Finally the fact that it is not yet a mature technology and doesn't offer capacities which can meet the needs of our application (they are used in the range

of mWatt), the extra cost and volume that the TFBs would add, it was decided not to be used.

Table 1.3: Comparison of Supercapacitors and Thin Film Batteries.

Manufacturer	Price (CHF)	Cap (F)	Voltage (V)	Esr (mΩ)	Volume (l)
Eaton Bussmann (SC)	6.84 CHF	35 F	2.7 V	20 mΩ	0.006 l

Manufacturer	Price (CHF)	Capacity (mAh)	Voltage (V)	$R_{\text{int}}(\Omega)$	Volume (l)	$I_{\max}mA$
ST Microelectronics (TFB)	30 CHF	0.7 mAh	3.9 V	100 Ω	0.005 l	10 mA
Infinite Power Solutions (TFB)	-	2.2 mAh	4.1 V	20 Ω	0.01 l	90 mA

Consequently, the optimal solution for the described application taking into consideration the cost, volume and power capabilities shown in the previous figures is exploiting only supercapacitors in a boost converter (Fig. 1.6(a)). In the following section, the design of the system is analyzed while the available commercial components are investigated.

1.4 Design of the Storage System

First the energy demands of the system are analyzed according to Fig. 1.2, Fig. 1.3 and Fig. 1.4 and then various supercapacitors are compared to conclude to the most appropriate one for the application.

The demands of the system are defined,

$$E_{\text{pulse}} = (36.25\ \text{W} - 1.25\ \text{W}) \cdot 1\ \text{s} = 35\ \text{J}$$

$$E_{\text{L}} = 15 \cdot E_{\text{pulse}} + P_{base} \cdot t_{\text{cycle}} = 15 \cdot 35\ \text{J} + 1.25\ \text{W} \cdot 22\ \text{s} = 552.5\ \text{J}$$

The above calculated Energy is based only at the Power profile of the load. For optimal design, the Energy of the harvester can also be computed, so that the stored energy based on the ESU Power will be excluded,

$$E_{harv} = \int_0^{22} 6.5 \cdot \left(1 - \frac{t}{22}\right)^2 - 1.5 = 14.67\ \text{J}$$

Therefore, the real Energy required for the storage system is

$$E_{store} = E_{\text{L}} - E_{\text{harv}} = 537.83\ \text{J}$$

Since $\frac{E_{harv}}{E_{\text{L}}} = 2.6\%$ during the discharging cycle, we can neglect the E_{harv} and consider this extra

energy a safe margin for tolerance and aging effects. The degradation of the capacitances will decrease the overall storage energy which would impose us to resize the system and move to larger capacitances to compensate these effects. So from now on it is considered that $E_{store} \approx E_L$ in order to increase the lifecycle of the designed system. Taking also into consideration the efficiency of the DC/DC converter during the discharging procedure, approximated as η_{boost}=*96%*, it is calculated that C_b structure must be able to be charged at

$$E_{charge} = \frac{E_{store}}{\eta_{boost}} = 575.5 \text{ J}$$

Furthermore, since the voltage at the bus is constant at 24V, the minimum capacitance of the total storage system is

$$E_{charge} = \int_0^{V_{bus}} C_{charge} \cdot V dV = \frac{C_{charge} \cdot V_{bus}^2}{2} \Rightarrow C_{charge} = 2 \text{ F}$$

This value C_{charge} is the minimum one in the case that we permit the full discharge of the capacitor during a cycle. Practically, we don't allow the supercapacitor to discharge all its energy for *efficiency* and *control* reasons but we set a minimum allowable voltage limit to $\sim \frac{V_{bus}}{2}$. This means that the available Energy storage of the capacitor should be offered to the load during the transition of the capacitor voltage from V_{bus} to $\frac{V_{bus}}{2}$

$$E_{charge} = \int_{\frac{V_{bus}}{2}}^{V_{bus}} C_{min} \cdot V dV = \frac{3}{8} C_{min} \cdot V_{bus}^2 \Rightarrow C_{min} = 2.67 \text{ F}$$

While the maximum available storage capability, so that the volume will be kept to minimum levels but also keep a safe margin due to aging and tolerance effects, is defined to

$$E_{max} \leq 2 \cdot E_{charge} \Rightarrow E_{max} \leq 1151 \text{ J}$$

which yields

$$2 \cdot E_{charge} = \int_{\frac{V_{bus}}{2}}^{V_{bus}} C_{max} \cdot V dV \Rightarrow C_{max} = 2 \cdot C_{min} = 5.33 \text{ F}$$

Taking also the tolerance of the capacitances of each Supercapacitor which is between ±20% and ±30% in most of them, it is needed to design a system with +30% available capacitance so that it will be possible to deliver the necessary energy. The following characteristics of the described storage system can be concluded,

$$575.5 \text{ J} \leq E_{C_b} \leq 1151 \text{ J}$$

$$21.6 \text{ V} \leq V_{C_b} \leq 2.64 \text{ V}$$

$$2.66 \text{ F} \leq C_b \leq 5.33 \text{ F}$$

$$3.46 \text{ F} \leq C_b(1 \pm 30\%) \leq 7 \text{ F}$$

$$t_{disch} = 22 \text{ s}$$

1.5 Supercapacitor Optimization

Significant parameters to our optimization are the

1. *Cost (CHF)*

2. *Volume (l)*

3. *Efficiency (%)*

of the total energy system.

The cost and the volume can be derived directly from the datasheet of the supercapacitors. As far as the efficiency is concerned a good approximation can be given by the following equation

$$1.\ \eta_{C_b} = \eta_{boost} \cdot \frac{E_{store}}{\frac{E_{store}}{n_{boost}} + \overline{P_{ESR}} \cdot 15 \text{ s}}$$

where the average loss in the capacitors during discharging is

$$2.\ \overline{P_{ESR}} = {I_{\text{RMS}}}^2 \cdot R_{\text{TOTAL\_ESR}}$$

And considering the current during discharge ($V_{bus} \longrightarrow \frac{V_{bus}}{2}$) as a linear function since we have small ESR and negligible current ripple,

$$3.\ I_{\text{RMS}} = \frac{\frac{P_L}{\eta_{\text{boost}}}}{V_{\text{bus}}} \sqrt{\int_0^1 (1+x)^2 \, \text{dx}} \approx \frac{\frac{36.25}{0.96}}{24} \cdot 1.53 = 2.4 \text{ A}$$

In Table 1.4 the basic values of all supercapacitors from Digikey and Farnell which are reasonable solutions (according to the assumptions of the previous section) for our project are shown. The $\frac{efficiency(\%)}{price(CHF)}$ versus the $\frac{\text{Energy density(J)}}{Volume(l)}$ curve is extracted so that the smallest and the most efficient supercapacitors are exhibited in 1.8.

Consequently the commercial available supercapacitors in Farnell and Digikey are compared. The sequence of preference is #28, #4, #3. The efficiency and the volume are computed for the whole system (∼9 supercapacitors).

Finally, it is worth to mention that only supercapacitors would be suitable for this application since the commercial capacitors have either very small values of capacitance like the Ceramic, Aluminium-Polymer and Film Capacitors which can't store the desired energy or are very expensive like the Aluminum ELCO from Vishay (MAL210146105E3 – 149 CHF per piece).

Table 1.4: Comparison of the most suitable Supercapacitors from Digikey and Farnell.

Nr	Manufacturer	Price (CHF)	C (F)	V_{nom} (V)	R_{ESR} (mΩ)	V_{tot} (l)	η(%)	E_{av} (J)
1	Eaton Bussmann HV1625-2R7256-R	4.25	25	2.7	27	0.0514	85.9	600.48
2	Eaton Bussmann HB1625-2R5256-R	4.88	25	2.5	40	0.0571	82.28	540
3	NessCap Co Ltd ESHSR-0050C0-002R7	6.19	50	2.7	14	0.095	88.8	1200.96
4	Eaton Bussmann HV1840-2R7606-R	7.09	60	2.7	18	0.0962	87.89	1440.72
5	Maxwell Tech. BCAP0050-P270-T01	7.16	50	2.7	20	0.095	87.44	1200.96
6	Eaton Bussmann HB1840-2R5606-R	7.76	60	2.5	25	0.1069	85.73	1296
7	NessCap Co Ltd ESHSR-0025C0-002R7	4.75	25	2.7	21	0.048	87.21	600.48
8	Eaton Bussmann HV1635-2R7356-R	6.17	35	2.7	24	0.0688	86.55	840.24
10	Eaton Bussmann HB1635-2R5356-R	6.98	35	2.5	30	0.0764	84.55	756
16	Nichicon JJC0E686MELC	13.56	68	2.5	60	0.3079	78.09	1468.8
17	Illinois Capacitor 256DCN2R7Q	5.4	25	2.7	30	0.0452	85.25	600.48
18	Elna America DZ-2R5D506T	23.6	50	2.5	80	0.2062	74.31	1080
19	Nichicon JUWT1826MHD	9.83	82	2.7	100	0.0962	72.56	1967.76
22	Nichicon JUMT1336MHD	8.43	33	2.7	100	0.0767	72.56	792.72
23	Taiyo Yuden PAS1840LA3R0506	19	50	3	70	0.0855	78.9	1350
24	Eaton Bussmann HV1850-2R7806-R	10.08	80	2.7	20	0.1374	87.44	1920.24
25	Nichicon JJC0E276MELB	11.24	27	2.5	90	0.1555	72.56	583.2
26	Nichicon JJC0E566MELA	12.49	56	2.5	70	0.2062	76.16	1209.6
27	Maxwell Technologies BCAP0025-P270-T01	4.72	25	2.7	42	0.0498	82.77	600.48
28	**Eaton Bussmann HV1245-2R7356-R**	**6.84**	**35**	**2.7**	**20**	**0.0499**	**87.44**	**840.24**
29	Nichicon JJC0E476MELZ	11.42	47	2.5	70	0.1597	76.16	1015.2
30	Nichicon JJC0E476MELA	11.78	47	2.5	70	0.1816	76.16	1015.2
31	Elna America DZN-2R5D506T	24.61	50	2.5	30	0.2062	84.55	1080

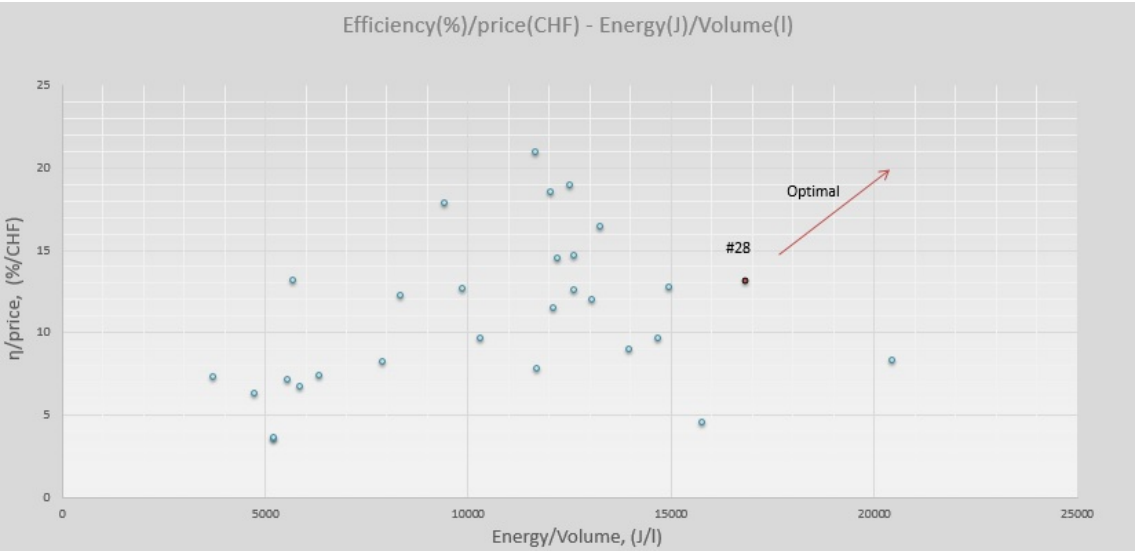


Figure 1.8: Efficiency versus Volume of Storage System.

1.6 Evaluation of the System

An arrangement of $n = 9$ supercapacitors in series of type #28 was chosen

$$C_{\mathrm{b}} = \frac{35F}{9} = 3.89 \text{ F}$$

$$V_{\mathrm{rated}} = 2.7V \cdot 9 = 24.3 \text{ V}$$

$$V = 0.05 \text{ l}$$

$$R_{ESR} = s \cdot 20 \ \cdot 9 \text{ m}\Omega \overset{s=1}{\Longrightarrow} R_{ESR} = 180 \text{ m}\Omega$$

$$Price = 6.84CHF \cdot 9 = 61.56 \text{ CHF}$$

$$E_{\mathrm{Cb\_charge}} = C_{\mathrm{b}} \frac{{V_{\mathrm{bus}}}^2}{2} = 1120.32 \text{ J}$$

$$E_{\mathrm{Cb\_av}} = 3 \cdot C_{\mathrm{b}} \frac{{V_{\mathrm{bus}}}^2}{8} = 840.24 \text{ J}$$

Remaining energy after breaking cycle in the capacitor can be computed as

$$E_{\mathrm{Cb\_after}} = E_{\mathrm{Cb\_charge}} - \frac{E_L}{\eta_{\mathrm{boost}}} - \overline{P}_{\mathrm{ESR}} \cdot 15 \ s \cdot 9 = \ 513.72 \text{ J}$$

This corresponds to a remaining voltage in the storage system

$$V_{\mathrm{Cb\_after}} = \sqrt{\frac{2E_{\mathrm{Cb\_after}}}{C_{\mathrm{b}}}} = 16.25 \text{ V}$$

In the worst case where the total capacitance will change by 30% and the ESR will increase by a factor of 2, the new values are extracted

$$0.7 \cdot C_{\mathrm{b}} = 0.7 \cdot \frac{35}{9} = 2.72 \text{ F}$$

$$V_{\mathrm{rated}} = 2.7 \cdot 9 = 24.3 \text{ V}$$

$$R_{ESR} = s \cdot 20 \ \cdot 9 \text{ m}\Omega \overset{s=2}{\Longrightarrow} R_{ESR} = 360 \text{ m}\Omega$$

$$E_{\mathrm{Cb\_charge}} = C_{\mathrm{b}} \frac{{V_{\mathrm{bus}}}^2}{2} = 783.36 \text{ J}$$

$$E_{\mathrm{Cb\_av}} = 3 \cdot C_{\mathrm{b}} \frac{{V_{\mathrm{bus}}}^2}{8} = 587.52 \text{ J}$$

$$\eta \approx 80\%$$

Remaining energy after breaking cycle in the capacitor can be computed as

$$E_{\mathrm{Cb\_after}} = E_{\mathrm{Cb\_charge}} - \frac{E_L}{\eta_{\mathrm{boost}}} - \overline{P_{ESR}} \cdot 15 \ s \cdot 9 = \ 177.62 \text{ J}$$

This corresponds to a remaining voltage in the storage system

$$V_{\mathrm{Cb\_after}} = \sqrt{\frac{2E_{\mathrm{Cb\_after}}}{C_{\mathrm{b}}}} = 11.43 \text{ V}$$

1.6.1 Balancing the Supercapacitors

Due to aging effects as well as temperature increase, the real value of the capacitors is changing and we have to take it into account for our system. The tolerance for the specific capacitance is ±30% which means that the Voltage across one capacitance can drop in the worst case up to

$$V_{Cb1} = 24\text{V} \cdot \frac{35\text{F} \cdot (1 - 30\%)}{35\text{F} \cdot (1 - 30\%) + 8 \cdot 35\text{F} \cdot (1 + 30\%)} = 1.5 \text{ V}$$

Or it can reach up to

$$V_{Cb1} = 24\text{V} \cdot \frac{35\text{F} \cdot (1 + 30\%)}{35\text{F} \cdot (1 + 30\%) + 8 \cdot 35\text{F} \cdot (1 - 30\%)} = 4.5 \text{ V}$$

The surge Voltage limit for the supercapacitance is up to 5.5V while the working voltage is 2.7V. To avoid such situations passive balancing techniques will be used. These consist of parallel placing in each Supercapacitor a resistor of the same value in order to keep constant the voltage drop in each cell. To choose an appropriate value of $R_{balance}$ the minimization of the charging time constant as well as the power losses on the resistance are considered. Thus,

$$\tau = R \cdot C = 35\text{F} \cdot R_{balance}$$

$$P_{losses} = \frac{(24V)^2}{9 \cdot R_{balance}} \leq 0.5 \text{ W}$$

where $C_{piece} = 35\text{F} \Rightarrow C_{tot} = 3.8\text{F}$ and considering a value $P_{losses} \approx 0.3\text{W}$, it is concluded that $R_{balance} = 220\Omega$

Finally one technique to compensate for variations in parallel resistance is to place a same valued bypass resistor in parallel with each cell, sized to dominate the total cell leakage current. This effectively reduces the variation of equivalent parallel resistance between the cells which is responsible for the leakage current.

1.6.2 Impact on generator

The power requirement for the generator is to charge the capacitor to V_{Cb}=24V within the startup charging time t_{ch}. Since the harvester power output is defined at 5W, the power available for the charging procedure is 5W-1.25W=3.75W and the charging time is computed

$$P_{\text{store}} \approx \frac{1}{\eta_{\text{boost}}} \frac{E_{\text{Cb\_max}}}{t_{\text{ch}}} \Rightarrow t_{\text{ch}} = 311 \text{ s}$$

And in the worst case because of capacitance degradation

$$t_{\text{ch}} = 218 \text{ s}$$

Chapter 2

Analysis of the Energy Storage Unit

In this chapter the operation of the Energy Storage Unit is described while an optimum design procedure of an inductor for the specific application is performed. The results of the storage components found in the previous chapter are summarized in the Table 2.1,

Table 2.1: Characteristics of the built system.

Manufacturer	Nr	Price (CHF)	C(F)	V_{Cb} (V)	ESR (mΩ)	Volume (l)	E_{Cb_av} (J)	η(%)	$V_{\text{Cb\_after}}$ (V)
Eaton Bussmann	9	61.56	3.89	24.3	180	0.050	840.24	89.72	16.25

while in the worst case (-30% of the nominal Capacitance)

Table 2.2: Characteristics of the built system in the worst case.

Nr	Price (CHF)	C(F)	V_{Cb} (V)	ESR (mΩ)	$E_{\text{Cb\_av}}$	η(%)	$V_{\text{Cb\_after}}$ (V)
9	61.56	2.7	24.3	360	588.2	80	11.43

In the following, the design of the boost converter is considered in order to size the components of the system since the output voltage must always be 24V while the input might fall up to 16V during the discharging cycle (and taking also into consideration the degradation of the SC in the worst case it might be 11.43V). The basic requirements are the sizing of the inductor of the DC-DC converter so that it operates in continuous conduction mode (CCM) which is ensured by the use of two transistors as well as $\Delta i_{Lb} \leq 20\% \cdot I_{Lb}$. Similarly the below analysis applies also for the buck converter during the charging stage.

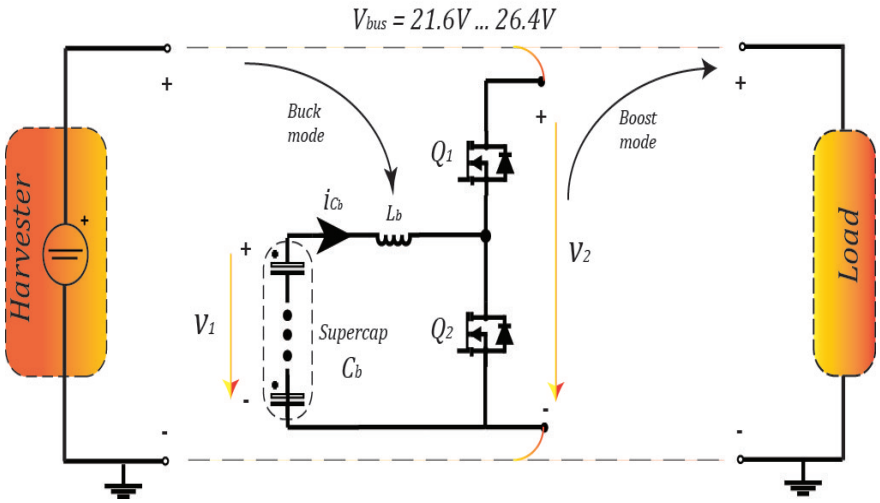


Figure 2.1: Overview of the designed System.

2.1 Analysis of the boost converter

In the beginning of the discharging cycle, it is assumed that the Capacitor storage system is fully charged at 24V. But as the supercapacitors are discharging the voltage over the storage system is falling, thus the use of a boost converter is imposed so that they can be able to deliver the required power to the load with a constant output voltage of 24V.

Table 2.3: Characteristics of the boost converter.

$V_1 = 11.43V...24V$	$V_2 = 24V$
$P_1 \approx P_2$	$P_2 = 36.25W$
$I_1 = I_L = \frac{I_2}{D}$	$I_2 = \frac{P_2}{V_2} = 1.5A$
$\Delta i_L = 20\% \cdot I_L$	
$D = \frac{V_1}{V_2} \Rightarrow 0.48 \leq D \leq 1$	

The voltage at the inductor will be,

$$V_L = L\frac{di}{dt} \approx L\frac{\Delta i_L}{(1-D)\cdot T_s} \Rightarrow$$

$$L = \frac{V_L \cdot (1-D)}{\Delta i_L \cdot f_s}$$

And by replacing

$$D = \frac{V_1}{V_2}, I_L = \frac{I_2}{D}, V_2 = 24V, V_L = \begin{cases} V_1, \ 0 < t < (1-D)T_s \\ V_1 - V_2, \ (1-D)T_s < t < T_s \end{cases},$$

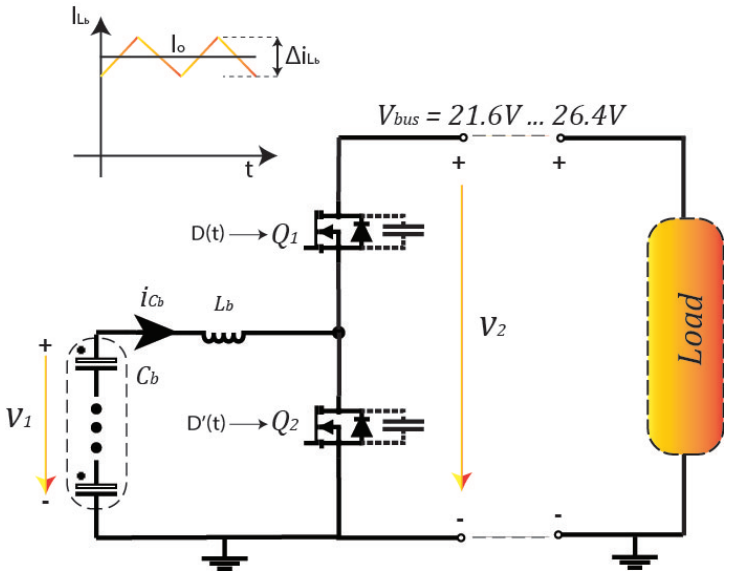


Figure 2.2: Boost converter.

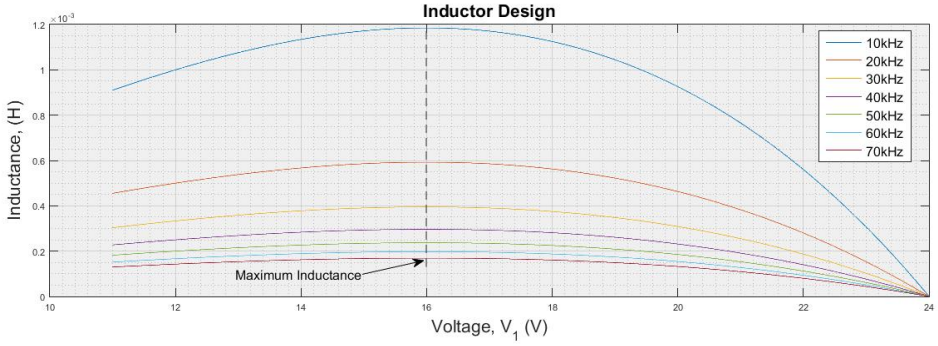


Figure 2.3: Inductor design.

it is derived,

$$L = \frac{V_1 \cdot \left(1 - \frac{V_1}{V_2}\right)}{0.2 \cdot \frac{I_2}{D} \cdot f_s} = \frac{V_1 \cdot \left(1 - \frac{V_1}{V_2}\right)}{0.2 \cdot \frac{1.5A}{\frac{V_1}{V_2}} \cdot f_s} \Rightarrow$$

$$\boldsymbol{L = \frac{-\frac{V_1^3}{24V} + V_1^2}{7.2 \cdot f_s}}$$

Where L is getting the maximum value for V_1=16V (Fig. 2.3). Consequently the worst case during which the largest inductance is needed is 16V.

Since the system is never in the steady state condition but the duty cycle factor changes continuously in relation with the bus and storage voltage, the design of the inductor must be done in the worst case so that the current doesn't become zero while the Δi_L is ensured to be $\leq 20\%$. The Δi_L is defined as the difference between the maximum and the minimum point of the Inductor current (Fig. 2.2).

Mosfet $Q1$	Mosfet $Q2$
$V_1 = 11.43V...24V$	
$V_2 = 24V$	
$I_2 = \frac{P_2}{V_2} = 1.5A$	
$D = \frac{V_1}{V_2} \Rightarrow 0.48 \leq D \leq 1$	
$V_{Q1}= -24V\ ,0 \leq t \leq (1-D)T_s$	$V_{Q2}=I_1 \cdot r_{DS}, 0 \leq t \leq (1-D)T_s$
$V_{Q1}=I_1 \cdot r_{DS}, (1-D)T_s \leq t \leq T_s$	$V_{Q2}=24V,\ (1-D)T_s \leq t \leq T_s$
$I_1 = I_{Lb} = \frac{I_o}{D} \Rightarrow 0 \leq I_1 \leq 3.13A$	
$\Delta i_L = 20\% \cdot I_1 \Rightarrow 0 \leq \Delta i_L \leq 0.6$	
$I_{RMS,Lb} = I_1 = \frac{I_o}{D}$	
$I_{Q1}=0, 0 \leq t \leq (1-D)T_s$	$I_{Q2}= I_1, 0 \leq t \leq (1-D)T_s$
$I_{Q1}=I_1, (1-D)T_s \leq t \leq T_s$	$I_{Q2}=0,\ (1-D)T_s \leq t \leq T_s$
$I_{max} = \frac{I_o}{D} + \frac{\Delta i_L}{2}, t = 0$	$I_{max} = \frac{I_o}{D} + \frac{\Delta i_L}{2},\ t = \ (1-D)T_s$
$I_{RMS,Q1} = \sqrt{\frac{1}{T} \cdot \int_{(1-D)T_s}^{T_s} I_1^2 dt} = \frac{I_o}{\sqrt{D}}$	$I_{RMS,Q2} = \sqrt{\frac{1}{T} \cdot \int_0^{(1-D)T_s} I_1^2 dt} = \frac{I_o\sqrt{1-D}}{D}$

The losses for the overall boost converter are computed below,

$$\boldsymbol{P_{Loss} = P_{Q1} + P_{Q2} + P_{Cb} + P_{Lb}}$$

It is worth to mention that during the boost mode, initially the transistor Q2 turns-on exhibiting hard turn-on which results in significant turn-on losses. The turn-on time was experimentally measured and can be seen in Fig. 2.4. Thus it was defined to 16ns result which is also consistent with the datasheet information. Concerning the turn-on of Q1, $P_{on,Q1}$ is considered ≈ 0 since when it switches on, the body diode of Q2 conducts leading to a zero current turn-on. Consequently, it is shown that the heating requirements for Q2 are larger compared to the first Mosfet since Q1 exhibit a soft turn-on.

On the other hand the turn-off losses can be neglected since the transistors exhibit soft turn-off behavior. This is achieved considering the parallel output capacitance (∼400pF) of the Mosfets which provide a zero voltage across the transistor while the current turns off resulting in zero voltage turn-off for Q1 and Q2.

Mosfet losses

$P_{Q1} = P_{Gate,Q1} + P_{COSS} + P_{cond,Q1}$	$P_{Q2} = P_{Gate,\ Q2} + P_{on,Q2} + P_{COSS} + P_{cond,Q2}$
Storage losses	**Inductor losses**
$P_{Cb} = P_{esr,Cb}$	$P_{Lb} = P_{Core,Lb} + P_{Cu,Lb}$

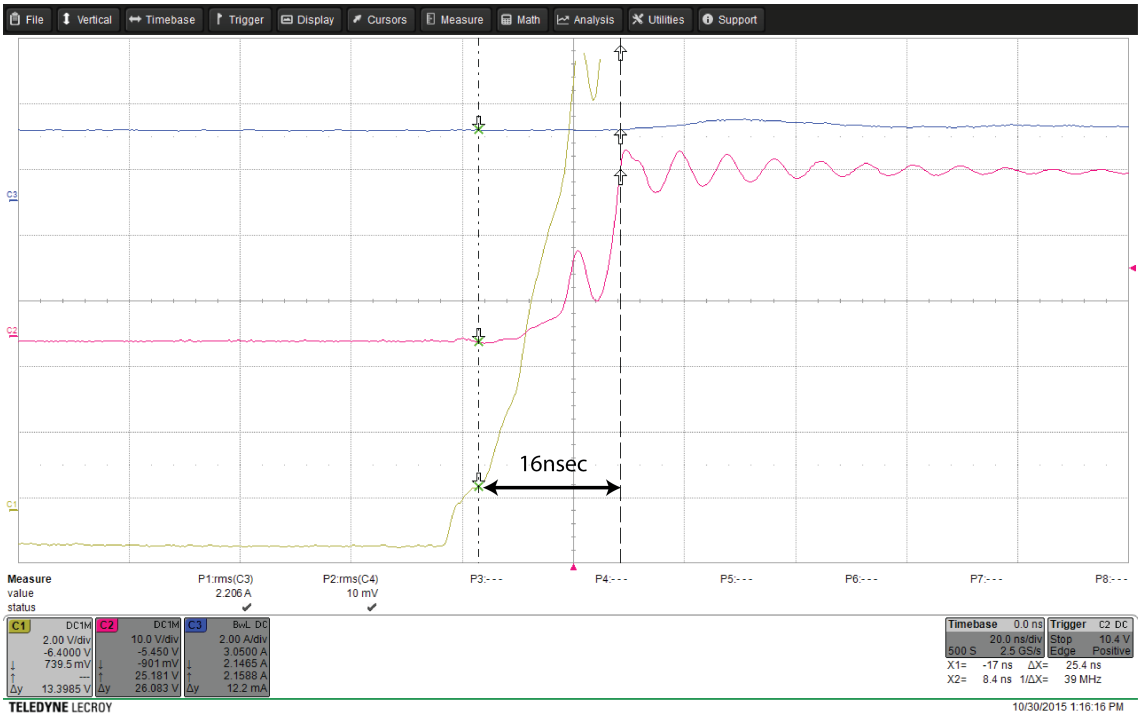


Figure 2.4: Turn-on Switching of the transistor.

And more specifically,

Table 2.4: Mosfet Losses

Gate Losses	$P_{Gate,Q1} = Q_G \cdot \Delta V_G \cdot f_s = 30nC \cdot (14-(-2))\text{V} \cdot f_s$ $P_{Gate,Q2} = Q_G \cdot \Delta V_G \cdot f_s = 30nC \cdot (14-(-2))\text{V} \cdot f_s$
Turn-on Losses	$P_{on,Q1} \approx 0$ $P_{on,Q2} = \frac{V_{Q2} \cdot I_{Q2}}{2} \cdot t_{on} \cdot f_s + Q_{rr} \cdot V_{Q2}$
Output Capacitance Losses C_{oss}	$P_{Coss} = \frac{C_{oss} \cdot V_o^2}{2} \cdot f_s$
Conduction Losses	$P_{Cond,Q1} = I_{RMS,Q1}^2 \cdot r_{DS}$ $P_{Cond,Q2} = I_{RMS,Q2}^2 \cdot r_{DS}$

Consequently considering the trade-off between optimization of efficiency and minimization of inductor volume (Fig. 2.5), a switching frequency of 50 kHz and an inductance of L=237μH is chosen.

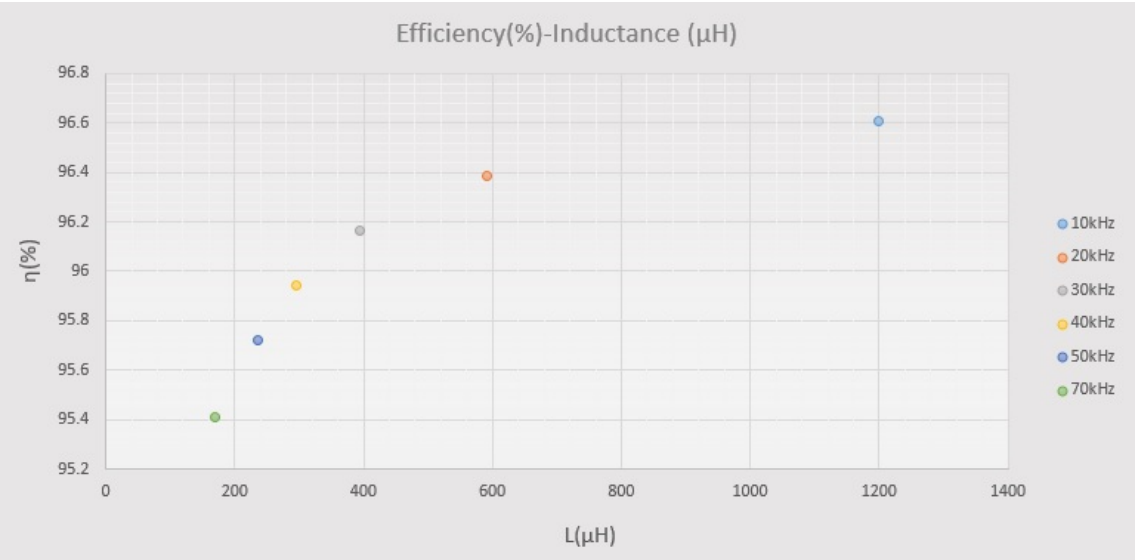


Figure 2.5: Efficiency versus inductance for various frequencies.

2.2 Inductor Design

Different approaches have been investigated in the literature how to size the optimum inductor. The most important ones are described in [1–3] by R.Erikson, T.Mohan and W.Kolar which are used on this document along with the GeckoMagnetics and MicroMetal software to find the best solution. In the end the derived designs of inductors as well as fixed value commercial ones are presented and compared.

The core selection must satisfy several constraints:

1. Must achieve the correct inductance
2. Keep the loss below a specified level
3. Keep the inductor size as small as possible without saturating the core

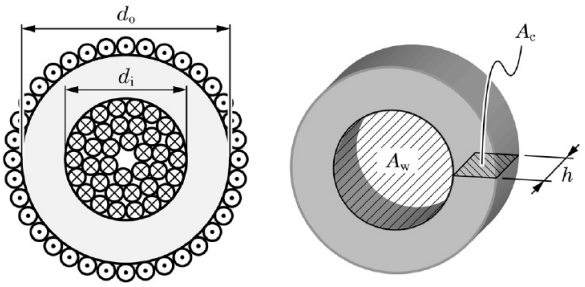
Specifications of the underlined project,

1. Wire resistivity: ρ_{cu} =1.724 $\cdot 10^{-6}$ $\Omega \cdot cm$ at room temperature
2. RMS winding current : $I_{RMS,Lb} = I_1 = \frac{I_o}{D} \Longrightarrow I_{max-RMS,Lb} = 3.1\text{A}$
3. Peak magnetizing current: $I_{pk,Lb} = I_{Lb,max} + \frac{\Delta i_L}{2} \approx \frac{36.25W}{11.43V} + \frac{0.6}{2} = 3.5\text{A}$
4. Calculated Inductance: L=250μH
5. Allowed copper loss: $P_{cu} \leq 1.5\text{W}$
6. Winding fill factor: $K_u \sim 0.3 \ldots 0.6$

7. Core maximum flux density: (according to the material)± 0.3T (Ferrite), 1.56T (Amorphous alloy 2605SA1)

2.2.1 Core of the Inductor

Firstly, the geometry of the core must be chosen. For simplicity, the analysis is done for toroidal inductors but it can be easily extended for other core types,



$$1.\ A_c = h\frac{(d_o - d_i)}{2}$$

$$2.\ A_w = d_i^2\frac{\pi}{4}$$

$$3.\ d_{i,min} = \left(\frac{LI_{pk}}{k_{lin}\pi B_{pk}A_c} + 1\right)\sqrt{\frac{I_{RMS}}{J_{RMS}}\frac{\pi}{4}}$$

Figure 2.6: Geometry of a toroidal core [3].

While the magnetic flux and the current density can be expressed in terms of the geometry of the core

$$4.\ B_{pk} = \frac{\Psi_{pk}}{NA_c} = \frac{LI_{pk}}{NA_c}$$

$$5.\ J_{RMS} = \frac{NI_{RMS}}{kA_w} = \frac{I_{RMS}}{d_{cu}^2\frac{\pi}{4}}$$

$$6.\ d_{i,min} = \frac{Nd_{cu}}{\pi}$$

So we conclude to the first limitation for the core dimensions,

$$7.\ A_c \cdot A_w \geq \frac{LI_{pk}I_{RMS}}{kB_{pk}J_{RMS}}$$

$$8.\ A_c \cdot d_{i,min} \geq \frac{LI_{pk}d_{cu}}{\pi B_{pk}}$$

B_{pk} is limited due to saturation of the core material while J_{RMS} is restricted to avoid excessive heat inside the coil. It is common to specify a certain maximum rms current density $J_{max} = 6\text{A/mm}^2$ which is valid approximation for an ambient temperature of 25^o Celsius and without any external method of thermal convection.

If a core with an air gap is chosen then it can be calculated by

$$9.\ l_g = \frac{\mu_o LI_{pk,Lb}^2}{B_{max}^2 A_c}\ \ (m)$$

The above equations reveal how the increase of the inductance or the peak current affect accordingly the core size. Increasing the flux density of the core allows a decrease in its size.

For the core saturation, an approximate method to see at which point of the B-H plot given by the manufacturer the inductor is operated is the use of the equation:

$$10.\ H = \frac{0.4\pi NI}{l_e}$$

$$11.\ B = \frac{LI_{pk}}{NA_c}$$

With this information it is possible to estimate from the B-H curves how significant will be the effect of the dc current and accordingly choose an appropriate effective magnetic path and core saturation limit. Ferrite cores exhibit hard saturation while powder cores soft one.

Two broad classes of materials are used for magnetic cores for inductors; alloys principally consisted of iron and ferrite cores. The first category exhibits greater flux density of up to 1.56T (like products from Rotima labeled from the trade name METGLAS) and the second one up to 400mT. Powdered iron cores belong to the first class and have low eddy current losses and thus can be used to higher frequencies.

2.2.2 Number of Turns and choice of material

The geometry limitations of the selected core are derived

$$12.\ N = \frac{LI_{pk}}{B_{pk}A_c}$$

But usually the manufacturer provides the inductance factor from which the turns can easily be derived

$$13.\ L = A_L N^2$$

2.2.3 Winding Type

Evaluation of the wire size which satisfies the following equation

$$14.\ A_{cu} \leq \frac{K_u A_w}{N_{min}}$$

2.2.4 Losses of the inductor and the winding

Winding loss is related to the wire guage and length (number of turns). Both of these parameters are constrained by the core geometry and thermal considerations.

Both the core and the wire contribute to the total losses

$$15.\ P_{Lb} = P_{Core,Lb} + P_{Cu,Lb}$$

As far as the core is concerned, the losses can be computed either from the P_V figures defined in

the datasheet by the manufacture

$$16.\ P_{core} = P_V \cdot V_e$$

Or by using the Steinmetz equation which is the method used usually by the inductor design software (e.g GeckoCircuits)

$$17.\ P_{core} = k_{core} f^n \Delta B^m V_e$$

$$18.\ \Delta B \approx \Delta I \frac{B_{max}}{I_{max}}$$

On the other hand, the wire losses are dependent by the number of turns and the magnetic length defined by the core size and material,

$$19.\ P_{Cu,Lb} = r_{Lb} \cdot I^2_{Lb,RMS}$$

$$20.\ r_{Lb} = \rho \cdot \frac{N \cdot MLT}{A_c}$$

2.2.5 Comparison of Inductors

In this section various commercial inductors are investigated with emphasis on the toroidal shape ones due to their small size and low inductances which are suitable for our application.

Digikey Cores

In the table below all the toroidal cores from Digikey can be seen. Only ferrite cores are available in this shape.

1. Required $A_c \cdot A_w \geq 0.5$ cm^4

2. Saturation limit $B_{sat} \leq 0.3$ T

3. Required turns, $N_{min} = \sqrt{\frac{L}{A_L}}$

If the saturation limit is exceeded then the designer should operate the inductor at a lower current or use a larger or even different core with an air gap or increase the number of turns.

Table 2.5: Commercial available toroidal cores in Digikey.

Unit Price (CHF)	A_L	**Material**	l_e **(mm)**	A_c **(mm^2)**	**Volume (l)**	N_{min}	$A_c \cdot A_w$ **(cm^4)**	**B(T)**	l_g **(mm)**	r_{Lb} **(mΩ)**
8.61	4.46µH	N87	120.4	195.7	0.045	8.2	13.83	0.65	2.07	75.42
15.13	12.6µH	T65	152.1	305.9	0.089	4.9	34.69	0.70	1.33	28.88
3.26	13.1µH	T38	73.78	76.98	0.012	4.8	2.18	2.84	5.28	112.237
3.37	5.46µH	N30	82.06	82.6	0.013	7.4	2.72	1.71	4.93	161.26
3.82	13.5µH	T38	89.65	95.89	0.018	4.7	3.98	2.33	4.24	88.22
11.66	5.4µH	N30	152.4	152.4	0.053	7.5	19.92	0.92	2.67	88.6
3.47	8µH	T37	89.65	95.89	0.018	6.1	3.98	1.80	4.24	114.5
10.64	5.4µH	N30	152.4	152.4	0.047	7.5	19.92	0.92	2.67	88.58
11.41	12µH	T37	120.4	195.7	0.045	5	13.83	1.07	2.08	45.98
2.77	5.75µH	N30	89.65	95.89	0.018	7.2	3.98	1.52	4.24	135.15
3.05	8.5µH	T37	73.78	76.98	0.012	5.9	2.18	2.31	5.28	137.95
12.17	7.16µH	T37	152.4	152.4	0.053	6.5	19.92	1.06	2.67	81.5
15.13	5µH	N87	152.1	305.9	0.089	7.7	34.69	0.45	1.33	45.3
16.44	10.8µH	N30	152.1	305.9	0.089	5.3	34.69	0.65	1.33	31.18
125.6	6.2µH	N30	375.8	458.9	0.385	7	382.35	0.33	0.88	27.45
261.97	5.2µH	N30	550.5	608.6	0.801	7.6	1118.90	0.23	-	22.47
32.9	5.5µH	N30	255.3	267.2	0.123	7.4	90.85	0.53	1.5	49.85
36.06	5.5µH	N30	255.3	267.2	0.14	7.4	90.85	0.53	1.52	49.85
4.56	3.59µH	N87	96.29	125.3	0.024	9.1	5.66	0.92	3.25	130.72

As can be seen only one core meet the saturation limit without the addition of an air gap ($B \leq B_{sat}$) but has a volume of 0.8 liter and 8 turns. It is a quite large inductor which is due to the core material. Ferrite cores, although they can offer low losses in high frequencies, have small flux saturation values which leads in high effective magnetic length and thus large inductors and ESR losses.

The inductors presented in Table 2.5 are the only commercially available from Digikey and Farnell suitable for our application considering the current limitations as well as the available quantities of the corresponding cores in Digikey. However, they exhibit quite large $A_c \cdot A_w$ values and an air gap is also needed to reduce the maximum flux saturation. The required air gap length (l_g in mm) is given based on Equation 9 while the theoretical calculated resistance of the wire (r_{Lb}) is computed according to Equation 20. Therefore in the following fixed value toroidal inductors are investigated from these suppliers as well as other core shapes.

Rotima Cores

Another option would be from a swiss supplier called Rotima which offers gapped toroidal cores with high saturation flux (∼1.56T).

1. Required $A_c \cdot A_w \geq 0.05$ cm^4

2. Saturation limit $B_{sat} \leq 1.5$ T

3. Required turns, $N_{min} = \sqrt{\frac{L}{A_L}}$

O.D. (mm)	**Ht (mm)**	**Volume (cm^3)**	**$A_c \cdot A_w$ (cm^4)**	**A_L(nH/N^2)**	**N_{min}**	**B(T)**
15.7988	3.18	0.345	0.055	27.37	104.7	1.11
17.4752	9.53	0.938	0.23	52.45	75.6	0.69
19.939	9.53	1.538	0.348	73.52	63.9	0.54
22.9616	9.53	2.382	0.494	95.38	56.1	0.44
25.5524	9.53	1.888	0.725	48.32	78.8	0.49
32.4358	9.53	5.336	1.21	119.56	50.1	0.30
34.925	9.53	5.577	1.77	97.49	55.5	0.29
39.9034	9.53	7.148	2.706	94.32	56.4	0.26
44.9072	9.53	9.91	3.472	111.99	51.8	0.22
44.67	14.19	10.918	6.17	101.11	54.5	0.20
55.2	13.79	15.127	11.376	88.74	58.1	0.18
31.5976	9.53	3.824	1.435	72.4	64.4	0.35

It is shown that for all the inductors the flux saturation limit is ensured. It is also noted that the turns needed are more than 50 for all the core sizes.

Custom Cores in GeckoMagnetics

Next analysis using the GeckoMagnetics is done for cores of other shapes

L (μH)	**Core type**	**Core Material**	**Wire**	**N**	**R_{dc} (mΩ)**	**Losses (W)**	**Volume (l)**	**Price (CHF)**
283.76	toroidal	Mega Flux 40u	AWG12	80	27.58	0.53	0.075	2.4
257.76	toroidal	Mega Flux 60u	AWG10	65	17.75	0.51	0.135	3.4
290.16	E55	N30+	AWG14	17	21.65	0.32	0.082	3.75·2
294.59	ETD 54/28/19 0.2 mm	N87+	AWG12	14	9.2	0.27	0.080	3.47·2
304.25	P 36x22 0.35mm	N87+	AWG14	21	21.51	0.34	0.022	6.2·2
290	RM 14 0.15mm	N87+	AWG12	15	9.4	0.25	0.026	5.6·2

Hence if other than toroidal core will be chosen, then the RM 14 with an 0.15mm air gap or the ETD 54/28/19 are the main candidate ones with very low losses and volume. These are available in Digikey. Take into account that the price is the double of it since two components are needed so that the according air gap will be formed.

Commercial Fixed Value Inductors and Conclusions

Finally, the fixed value conductors available in Digikey are compared with the previous custom cores. The optimal solution is displayed in Fig. 2.7. On this figure, the efficiency is derived as a function of $\eta \sim \frac{1}{DCR(m\Omega)}$. Therefore, it is assumed that the leading factor for higher efficiency is the ohmic resistance in the core and the wire.

Table 2.6: Optimal Inductor.

Digi Key	Price (CHF)	Material Core	Inductance (μH)	Current Rating (A)	ESR (mΩ)	Volume (l)
M8379-ND	7.65	Ferrite	220μH	7.4A	50mΩ	0.03

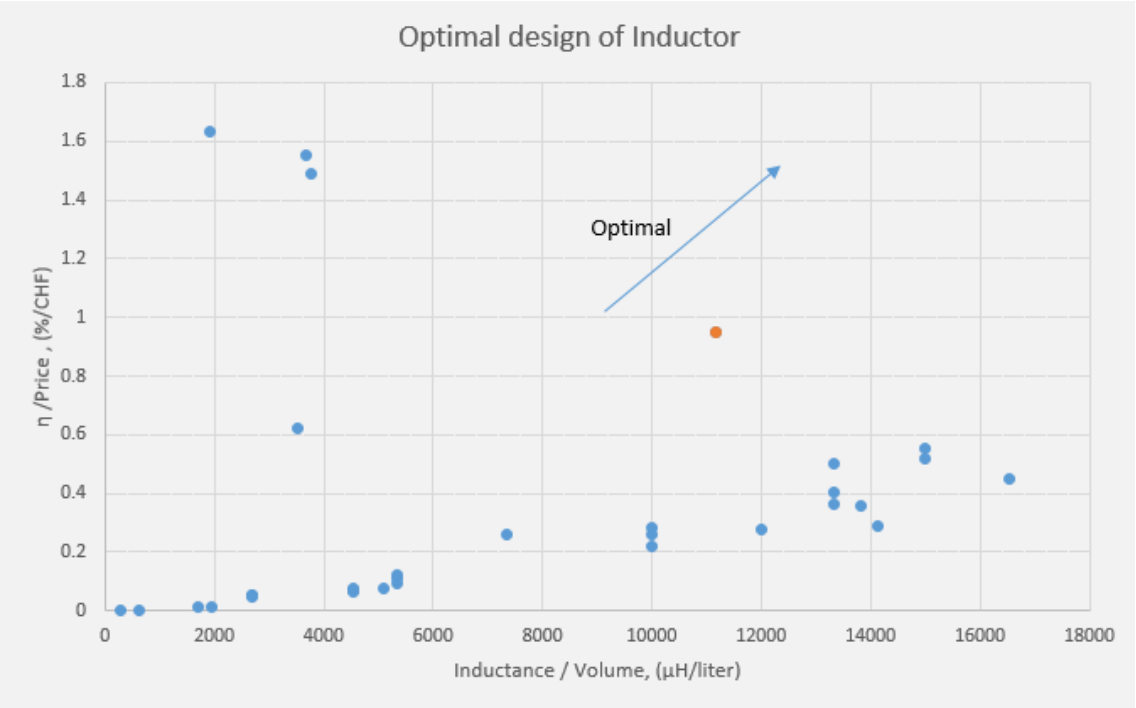


Figure 2.7: Optimal design of inductor.

It is shown in the plot that the selected inductor has the best relation $\frac{Inductance(\mu\text{H})}{Volume(\text{l})}$ and $\frac{Efficiency(\%)}{Price(\text{CHF})}$ at the rated current of our application $I_{rated} \leq 4\text{A}$. According to the Datasheet, this inductor at its saturation current $I_{sat} = 7.4\text{A}$ has an inductance of $220\mu\text{H}$. The losses are $P_{Cu,Lb} = r_{Lb} \cdot I^2_{Lb,RMS} < 0.05 \cdot 3.1^2 = 0.48\text{W}$. Consequently taking into consideration efficiency, volume, cost and construction simplicity it is derived that the optimal inductor for the described application is a fixed one with characteristics given in Table. 2.6.

Chapter 3

Implementation of the Control Scheme

The demands for the proper operation of the designed harvesting system are to keep the bus voltage constant to 24V and absorb the required power from the harvester in order to be able to deliver to the load the power needed according to its profile. To achieve such operation a control scheme is needed to modify the output of the DC-DC converter. Adding a closed-loop feedback to the converter will hold the output voltage at a set point by automatically adjusting the duty cycle control signal to the MOSFETs.

3.1 Overview

In Fig. 3.1, the various stages of the system are displayed. With a blue arrow the charging operation is shown where the harvested power is transferred to the storage unit. During the discharging period the power is delivered to the load (green arrow).

In the first stage, as long as the harvester pushes power to the bus voltage the ESU tries to regulate the V_{bus} to 24V by storing the energy to the supercapacitors. When they are fully charged and cannot absorb any more energy, an increase in the bus voltage $V_{bus} > 24$V will be noticed. Thus, the harvester stops operating and the ESU starts to discharge the supercapacitors. They are discharged in a way so that the bus voltage is stabilized to 24V.

In order to satisfy the above requirements a PI control scheme was developed to adjust the duty cycle as necessary, to obtain the desired output voltage with high accuracy regardless of load and voltage variations.

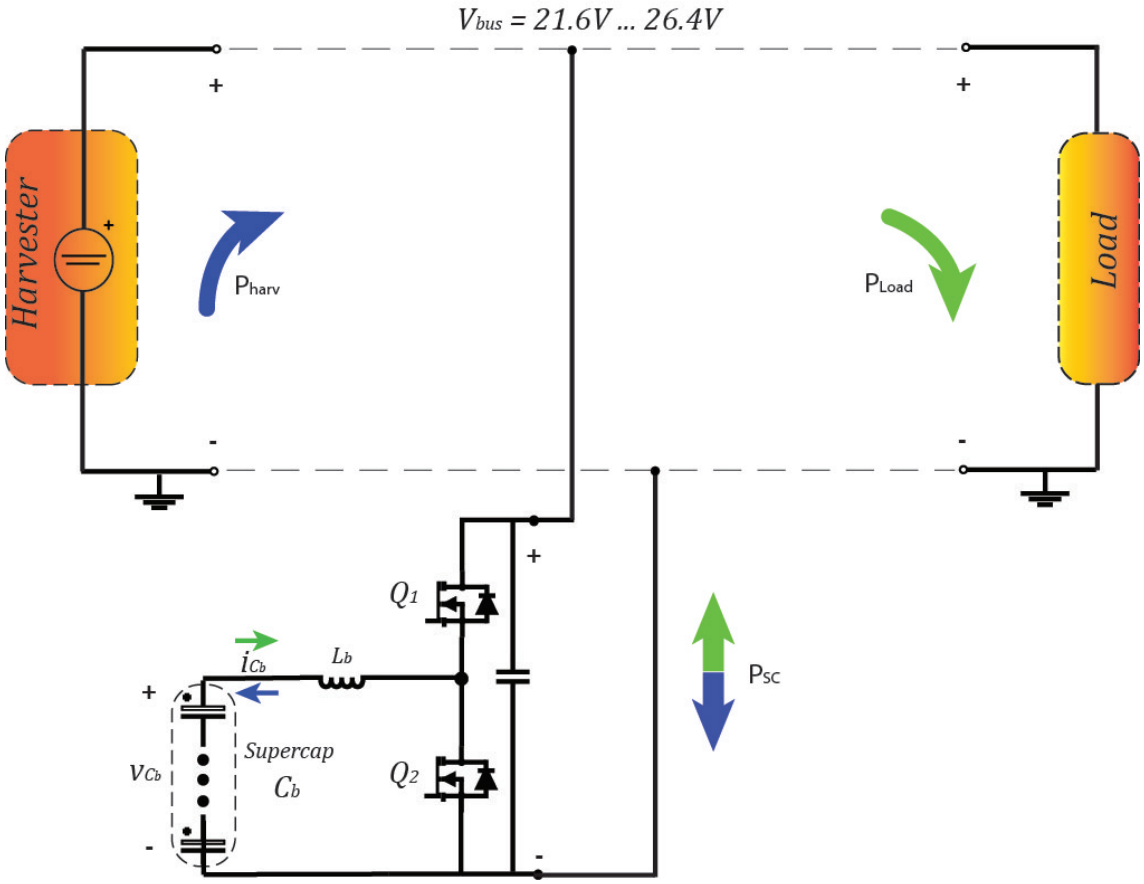


Figure 3.1: Overview of the System structure.

3.2 PI Control Scheme

A reference voltage of 24V is constantly compared with the output and creates an error signal which consists the input value of the PI controller. After properly tuning the PI values, the duty cycle will be derived and will provide the PWM input signal to the gate drives of the transistors.

PI controller is used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.

The PI controller converts the difference in the digital set-point and the digital output of the averaging block into a digital output control signal. This digital value is converted to a pulse-width modulated (PWM) signal by the micro controller so that the converter control input will vary regardless the supercapacitor voltage and the output voltage will be equal to the reference value.

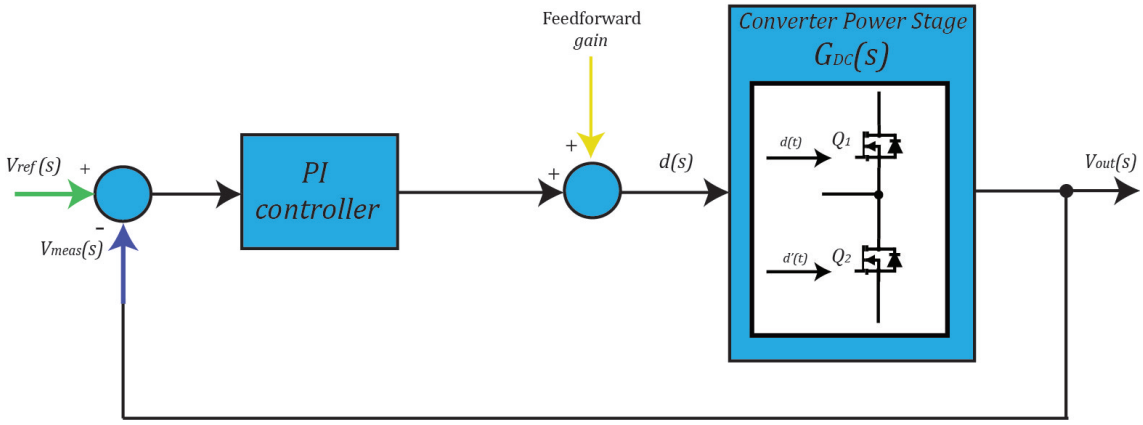


Figure 3.2: PI control scheme.

$$V_{error}\,(t) = V_{ref}\,(t) - V_{meas}\,(t)$$

$$d(t) = K_p \cdot V_{error}(t) + K_i \cdot \int_0^t V_{error}(\tau)d\tau) + \text{FeedForwardGain}$$

Although the open-loop system is stable (but with a high steady state error), the addition of a negative feedback loop might make it unstable. Thus, special attention should be given in the correct sizing of the terms.

In order to find out the value of K_p and K_i the manual tuning technique of Ziegler-Nichols step response method was used. It is performed by setting the I (integral) gains to zero and increase the K_p gain until it reaches the value K_u, at which the output of the control loop has stable and consistent oscillations. K_u and the oscillation period T_u are used to set the P and I gains. Thus $K_p = 0.020$ and $K_i = 10$.

It is worth to mention that the addition of a Derivative term is not necessary on the specific application since it doesn't improve very much the settling time and the overshoot of the bus voltage but it adds more complexity and processing time for the micro controller.

During the charging stage the $V_{Cb} = D \cdot V_{bus} \rightarrow D = \frac{V_{Cb}}{24\text{V}}$. By adding a Feedforward Gain $= D$ in the PI output, the rise time of the bus voltage is increased in both operations which is also justified by the simulations.

3.3 Simulations

In order to verify the above results, simulations in GeckoCircuits were done and are displayed below. Due to the large demands in processing power the simulations were separated in buck and boost operation.

3.3.1 Charging stage

The harvester may be simulated as a constant voltage source of 26.4V output and 11.43Ω internal resistance.

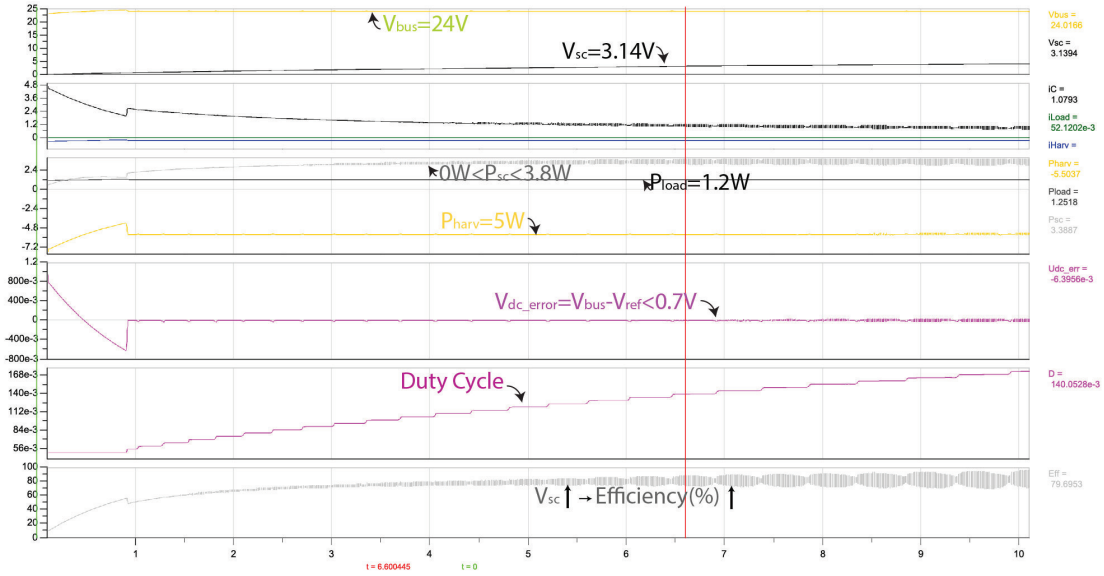


Figure 3.3: Charging cycle during the first 10 seconds.

Table 3.1: Charging characteristics for the first 10 seconds

P_{harv}	5.5 W
P_{sc}	3.3 W
P_L	1.25 W
η_{ch}	78%
$\lvert V_{bus-error}\rvert$	$\leq$ 0.7 V

As was explained in the first chapter, the storage unit in order to be fully charged needs approximately $\approx$ 300 seconds which is not possible to be simulated. Thus two figures are displayed; the first one is from the first 10 seconds and at the second one V_{sc} was initialized at 22V.

Table 3.2: Charging characteristics when $V_{sc0} = 22V$.

P_{harv}	6 W
P_{sc}	4 W
P_L	1.3 W
η_{ch}	85%
$\lvert V_{bus-error} \rvert$	$\leq$ 0.4V

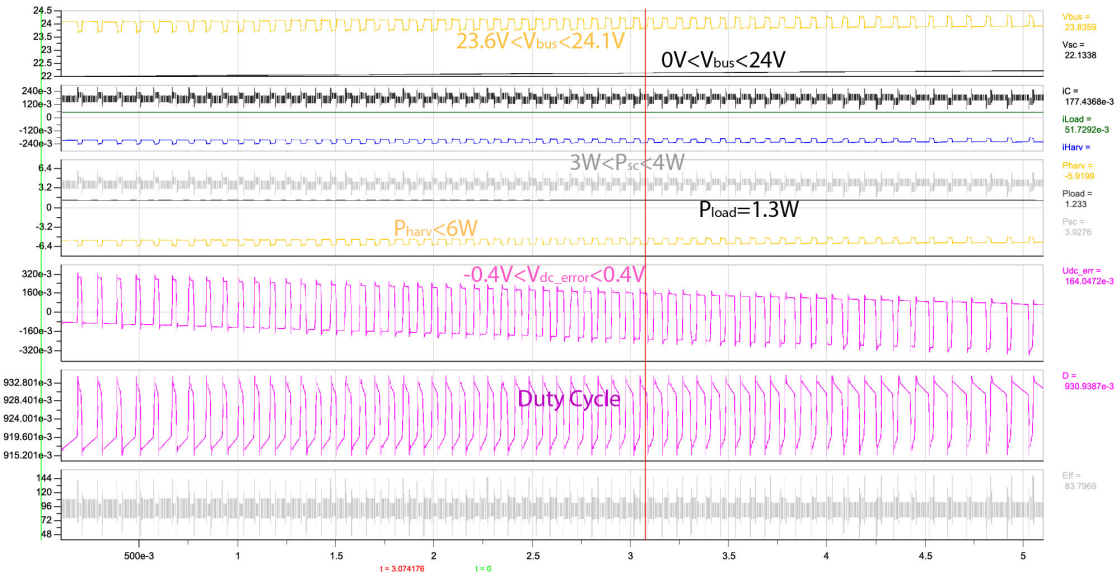


Figure 3.4: Charging cycle with $V_{sc0} = 22$V.

In both figures, it can be easily seen that the bus voltage remains constant at 24V while the error $V_{bus-error} = 24\text{V} - V_{bus}$ remains below of 0.32V. The efficiency of the charging cycle is also depicted in the last plot where $\eta = \frac{P_{SC}}{P_{harv} - P_L}\%$. This value is highly dependent by the voltage in the Supercapacitors and as it is growing, the same also applies for the overall efficiency. So, in the beginning a large amount of power is consumed in the internal ESR of each cell but as the voltage across it continues to increase, it is used for the charging of the storage unit.

Finally, it is noted that the optimum way to charge the Supercapacitors is by providing maximum power transfer from the harvester to the ESU. This may happen by applying almost constant current with an exponential increasing voltage until it reaches 24V point at which the current is falling to keep the absorbed power constant.

Table 3.3: Overall charging characteristics.

t_{ch}	310 sec
P_{harv}	5W
P_{sc}	$\leq$ 4 W
P_L	1.25 W
η_{ch}	$\geq$ 75%
$\lvert V_{bus-error} \rvert$	$\leq$ 1V

3.3.2 Discharging stage

During the discharging stage, the load is simulated by a load varying between 1.25W and 36.25W with constant bus voltage. Thus the ESU must be able to provide the corresponding current.

In the first figure, the overall behavior of the control scheme for the first 10 seconds are shown. The signal ENload implements the transition of the load from a low value to a high one by changing the output resistor connected to the bus. At this operation scheme, the error bus voltage satisfies the $\pm 10\% \cdot 24\text{V}$ voltage margin through the whole cycle.

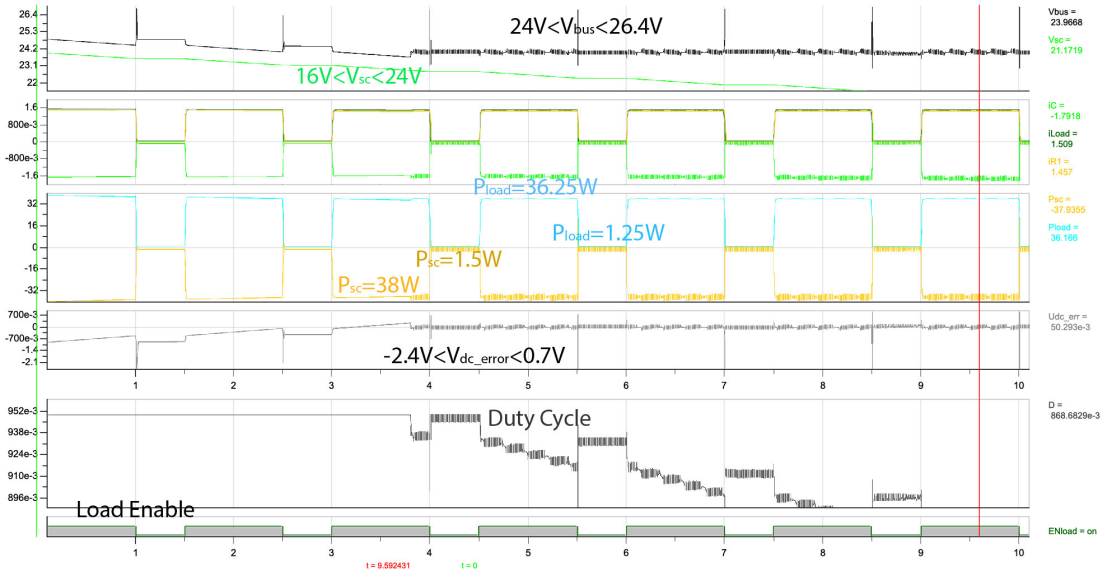


Figure 3.5: Discharging cycle during the first 10 seconds.

Table 3.4: Discharging characteristics for the first 10 seconds.

P_{sc}	38 W
P_L	36.2 W
η_{disch}	95%
$\lvert V_{bus-error} \rvert$	$\leq 2.4V$

Table 3.5: Dynamics of Supercapacitor Power and Voltage bus.

SC Power dynamics		Voltage dynamics	
P_{sc}-$t_{rise-time}$	12ms	V_{bus}-$t_{rise-time}$	300μs
P_{sc}-$t_{fall-time}$	600μs	V_{bus}-$t_{oscillations}$	2.3ms

The previous argument can also be verified in Fig. 3.6. where the voltage oscillations of the bus is below 2.4V in the worst case. It is also shown that despite the decrease of the storage voltage, the output remains constant to 24V with no sifnificant variations. Finally, the efficiency of the discharging cycle is also kept in high levels ($\geq$ 90%) and is restricted only by the ESR of the capacitances and the parasitic elements of the system.

Table 3.6: Voltage and current variation during the transition of P_L from 36.25W to 1.25W.

$V_{bus-max}$	26.4 V
P_{sc}	38 W
P_L	36.2 W
η_{disch}	95%
$\lvert V_{bus-error} \rvert$	$\leq$ 2.4V

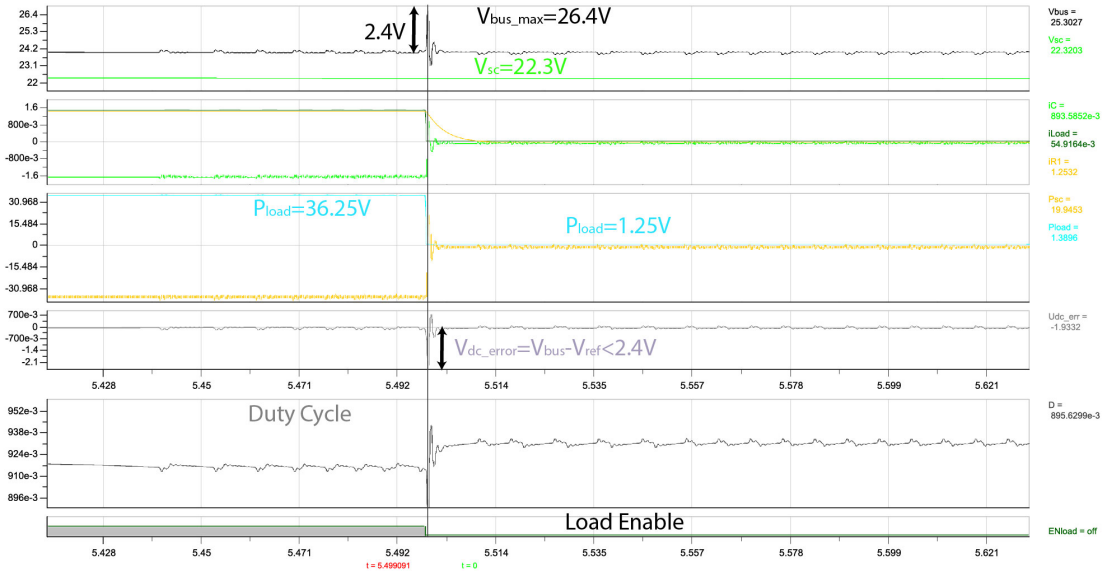


Figure 3.6: Zoom in the oscillations of the discharging cycle.

During this chapter, the PI scheme was explained while manual tuning of its terms in Gecko-Circuit was performed in order to extract the most appropriate values. The results were evaluated by the last figures which confirm the capability of the algorithm to modify the input duty cycle and consequently the bus voltage despite any voltage disturbances.

Table 3.7: Overall dsicharging characteristics.

t_{disch}	22 s
P_{sc}	$\leq$ 38 W
P_L	$\leq$ 36.5 W
η_{disch}	95%
V_{bus}	$\leq$ 26.4 V
$\lvert V_{bus-error} \rvert$	$\leq$ 2.4 V

Chapter 4

Hardware and Software Implementation

In the final chapter, the storage unit and its final PCB design are presented while the software of the selected control scheme is analyzed and implemented with a micro controller. Finally, the experimental setup is explained and the operation of the system during a charging cycle is shown.

4.1 Hardware Implementation

In this section the storage unit that was designed in the first two chapters is implemented in ALTIUM PCB design in order to extract a PCB circuit. The components that were used are the following

Table 4.1: Components of Storage Unit.

Component	Nr of Components	Volume (l)
Eaton Bussmann (SuperCap)	×9	0.05 l
M8379-ND (Inductor)	×1	0.03 l
Cap 1210 X7R (Capacitor)	×4	4×10^{-5} l
Res 1206 (Resistor)	×9	6×10^{-6} l
Total Volume		0.18 l

For simplicity reasons only the bottom layer was used while its size was designed to match the DC/DC Converter Prototype used in this application designed by M. Flankl. Finally, the PCB circuit of the designed storage unit is displayed in Fig. 4.2.

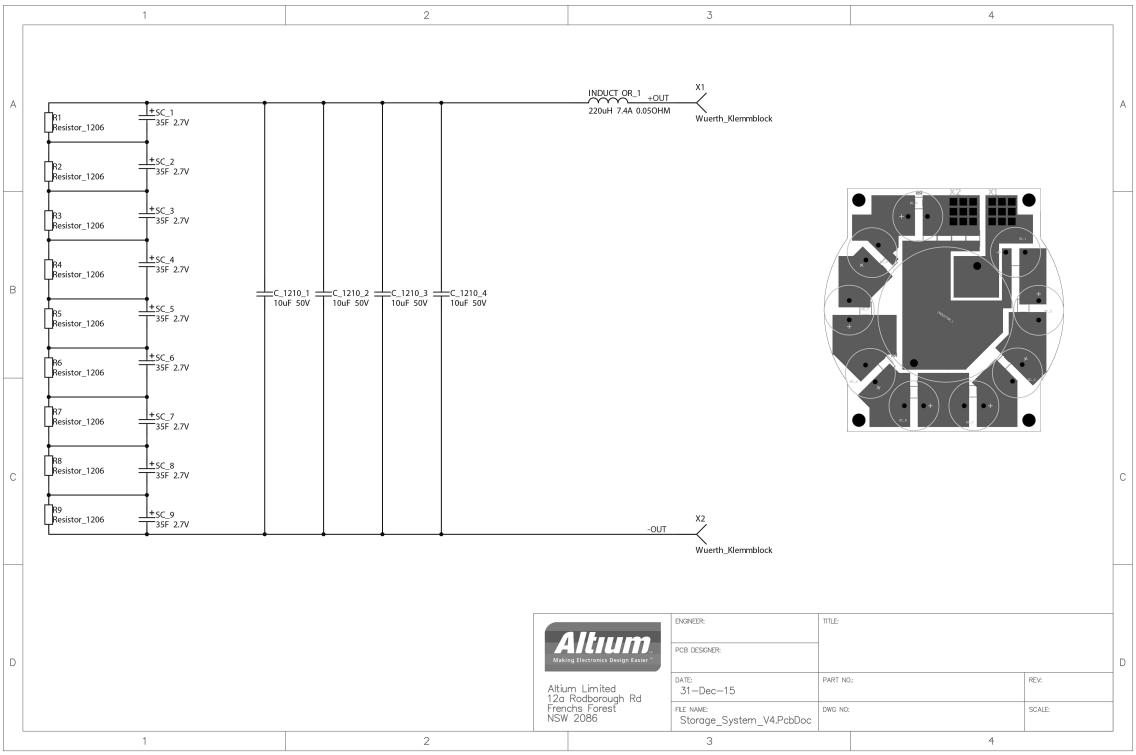


Figure 4.1: Hardware design in Altium.

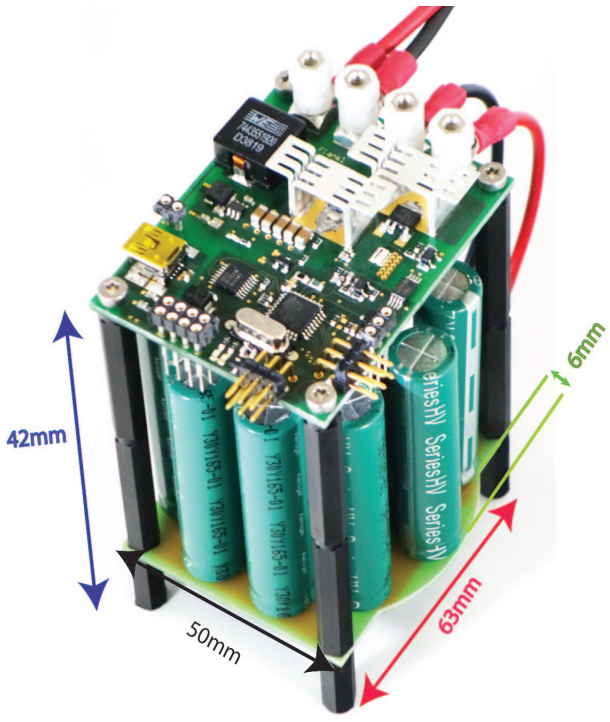


Figure 4.2: PCB design of the storage unit.

4.2 Software Considerations

For the implementation of the control scheme the ATMEGA88PA was used. It is an 8-bit processor and the software follows the flow diagram in Fig. 4.4. It should be pointed out that low-cost micro-controllers have considerable hardware limitations which mean that although control theory offers great tools to adjust the output values, in practice we are restricted by the capabilities of the processor power. In this section, the limitations occured during the programming of the device are exhibited and analyzed.

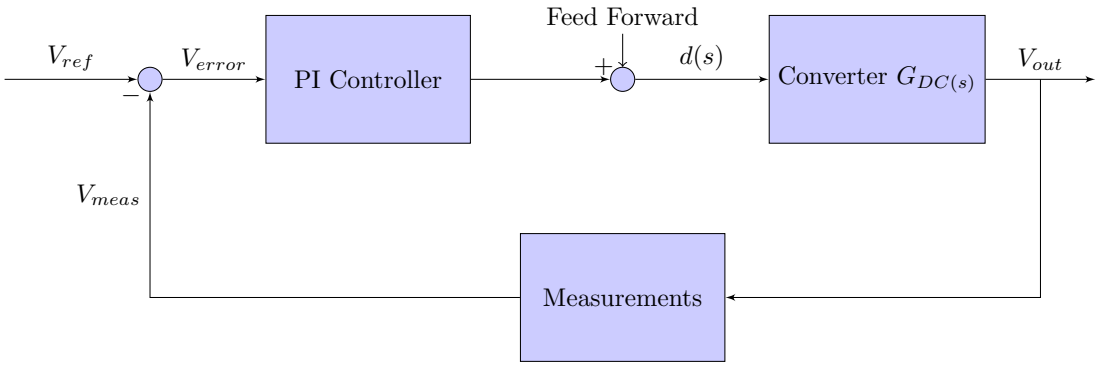


Figure 4.3: PI scheme implemented in ATMEGA88PA.

The code is based on the use of internal interrupts. The reading of the ADC values happens every 128kHz while the PI control takes place every 4kHz. The reading of the analog values so often consists a requirement of the specific micro controller while the modulation factor $d(t)$ updates with a period of 250μs. There is no need in a faster refresh of the K_p and K_i values since this would increase the bus voltage oscillations.

After the update of the PI scheme, it is needed to check if the Integral term has reached a maximum value. This is a known problem called Integral windup and occurs as a limitation of physical systems compared to ideal ones. It is a situation where the I term accumulates a significant error mainly caused due to excess overshoots. If it reaches this value, then it must be re-initialized since the system might become unstable and return to the reference state in a slower way. Consequently, it is needed to prevent the integral term from accumulating above or below predetermined bounds and constrain the process output within feasible margins.

Furthermore, the PI values computed before in Laplace form need to be discretized in order to input them in the algorithm. Considering that the sampling period used is 4kHz, it is concluded that

$$K_p = 0.020 \frac{\text{digits}}{\text{Volt}}$$

$$K_i = 0.0025 \frac{\text{digits}}{\text{Volt}}$$

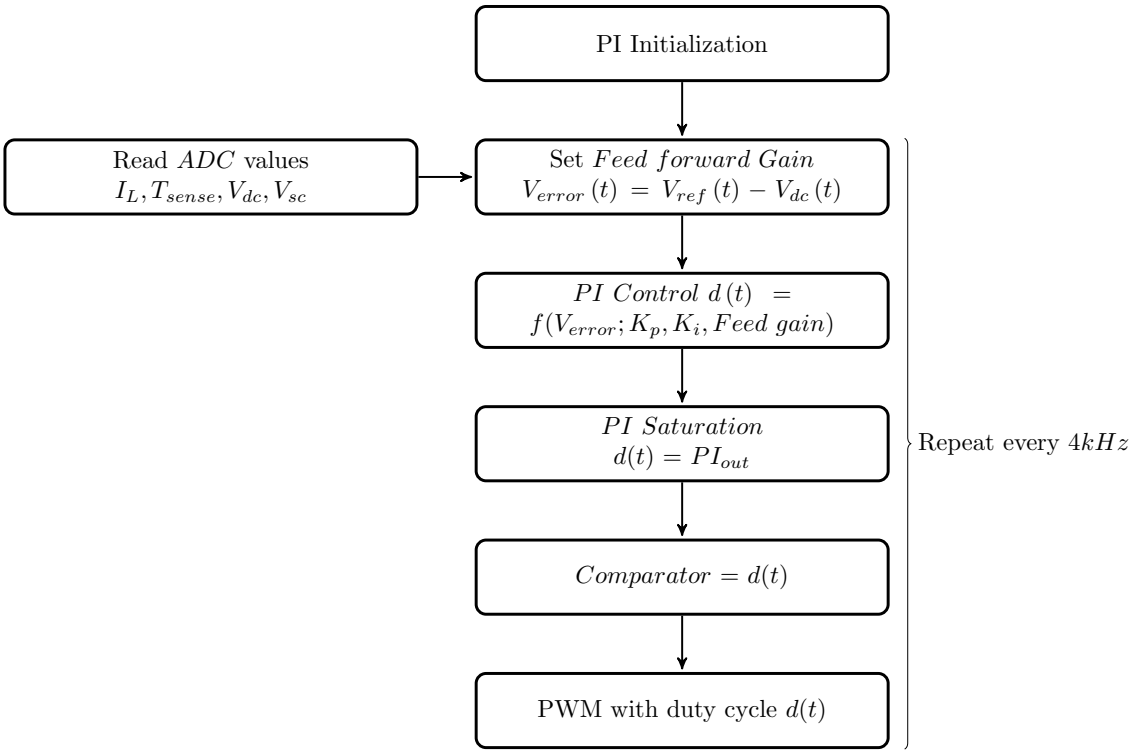


Figure 4.4: PI control software scheme.

Since the ATMEGA88PA features an 8-bit ADC input, it means that each analog signal is translated to a value between 0 and $2^8 - 1 = 255$. As the voltage which is permitted in the ADC inputs is 5V, after experimental verification it was found that each volt corresponds to ≈ 17 digits. As will be shown later, the ADC inputs may read large spikes which make it difficult to know the real value of the device. Thus, the last values of the specific ADC input are kept in order to extract the average and neglect the large overshoots. Another way to remove the spikes is to use the ADC noise canceling of the micro controller but this would increase a lot the run time of the algorithm since the processor must go to idle mode.

Additionally, during the programming of the device, it was preferred to use integer numbers instead of float ones since it would result in a much slower running time. However, integer values reduce the output accuracy of the duty cycle. Hence all numbers need to be converted to integer ones while the output of the PI algorithm are allowed to have a value between $10 - 245$ digits. Special attention must to be given to overflow problems during the calculation of the PI terms.

In the final step, the output of the PI controller is the duty cycle and is assigned to a comparator register in order to produce a PWM signal for the gate drive of the transistors. Another limitation was noticed on this point since the production of a correct-phase PWM signal of 50kHz was possible only if we wanted to sacrifice the accuracy. This happens because in order to create a 50kHz signal, it is needed to use a prescaling factor to reduce the external clock frequency. In addition to this, it is also required to use the Comparator Register 1 (OCR1A) and change the TOP value that it

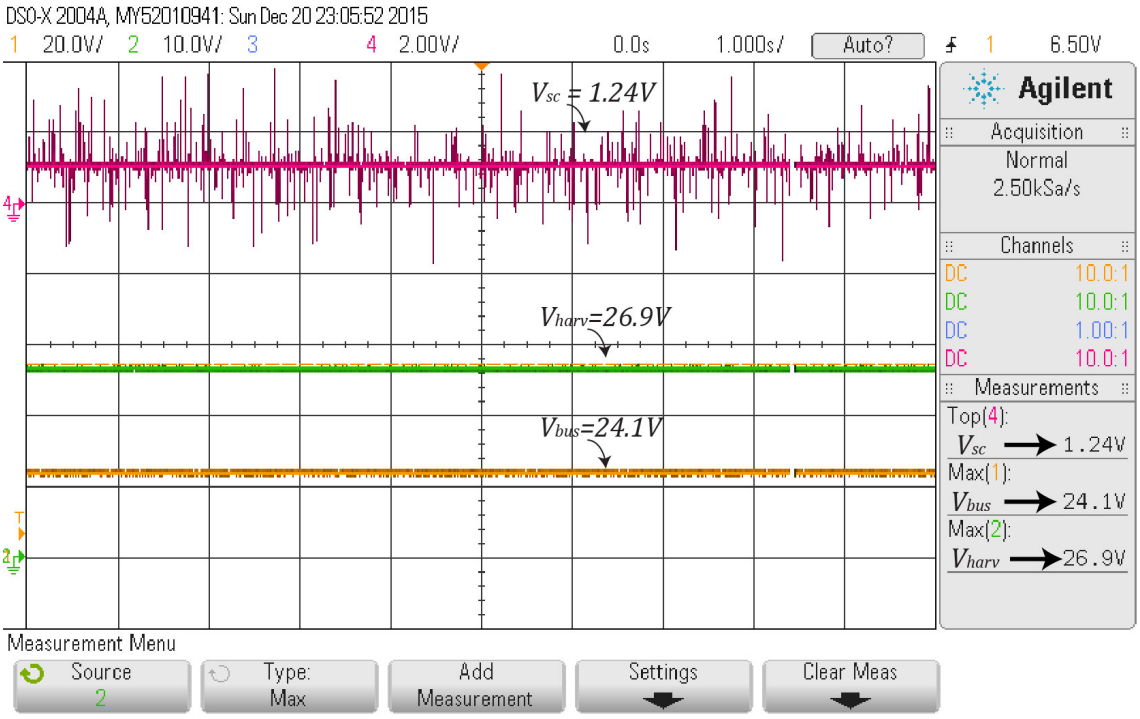


Figure 4.5: Voltage waveforms during charging.

can reach and therefore not fully exploiting its capabilities and reducing output accuracy. Thus, it was preferred to implement a fast PWM signal of 64kHz. Since the output signal will be used in a DC-DC operation and not for AC conversion a fast PWM signal doesn't influence the operation.

4.3 Experimental Results

In this section a rough application of the implemented PI scheme is implemented. In the same way that the charging and discharging stages were separated in the simulations, the following figures refer to the charging state. As a harvester a constant voltage source of $\geq$ 25.5V was used while in order to simulate the constant power but also protect the ESU a series power resistor of 50Ω was placed to the system. In Fig. 4.5, it is verified that the PI controller is working properly since the bus voltage is kept constant to 24V even though 26.9V are provided by the source. It is also noticed that the Supercapacitor voltage present a lot of spikes which are not real but are due to the problematic reading of the ADC inputs. In order to evaluate the cycle efficiency, the Fig. 4.6 was extracted where the current of the Supercapacitors is plotted. Since the current provided by the source is constant and equal to 0.2A the harvester power may be considered P_{harv} = 25.4V·0.2A= 5W while the P_{sc} = 24V·0.182A·9 = 3W which is not very efficient (75%) but as the voltage in the supercaps is increased so does also the efficiency. In the above plots the capability of the ESU to keep the bus voltage constant is proved. As long as the constant voltage source provide a voltage which is greater than 24V, the PI controller adjust the voltage

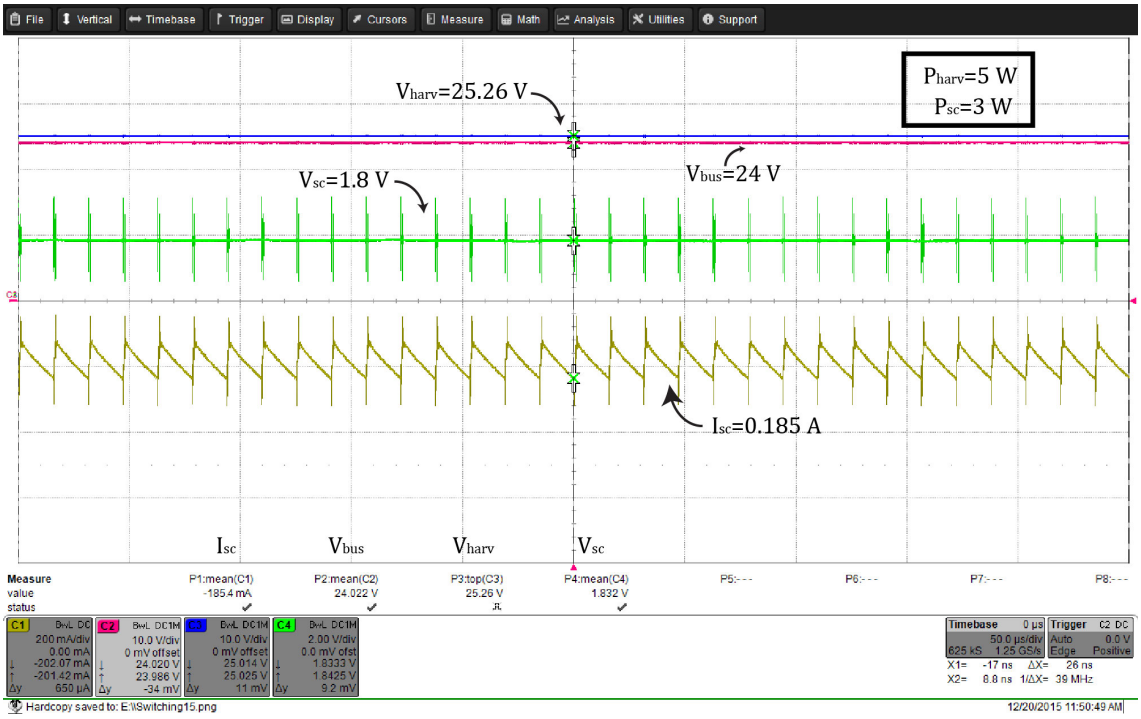


Figure 4.6: Voltage and Current waveforms during charging.

output of the converter and maintain the bus voltage in constant levels. Following the simulation results in Geckocircuits ($\eta_{ch} \geq 78\%$ depending the voltage in the supercapacitors), it is exhibited that the experimentally measured charging efficiency is 75%. However, further research should be done in order to simulate better the harvester and provide higher power and succeed better cycle efficiencies.

Table 4.2: Experimental results

V_{harv}	25.4 V
I_{harv}	0.2 A
V_{sc}	1.8 V
I_{sc}	0.185 A
V_{bus}	24 V
V_{error}	$\leq$ 1 V
P_{harv}	5 W
P_{sc}	3 W
η_{ch}	75%

To sum up, the PCB design of the storage unit was implemented and a PI control scheme was presented. The challenges that were faced during the programming of the micro controller were explained while the use of integer values instead of float numbers which were used during the simulations introduced problems in the accuracy of the PI output. Hence, it was necessary to re tune and modify a little the terms in order to achieve the desired stable output. Finally, it is concluded that the realization of the control scheme was able to keep the bus voltage constant during the

charging cycle exhibiting satisfactory results while they were consistent with the simulations in the previous chapter.

Chapter 5

Conclusions and Outlook

According to the given analysis, an optimum storage unit and inductor was designed and realized in terms of cost, volume and efficiency. A PI controller along with the designed storage unit exhibited a good perfomance since it was succeeded to keep constant the bus voltage regardless the input disturbances while the output results were validated both from the simulations and the experimental setup.

Concerning the control algorithm, a further optimization might be achieved by using a different scheme. A cascaded voltage and current loop control could be used for further stability and faster response to voltage and power variations. However, limitations with the current measurement prevented an implementation in the course of this project. Moreover, an improved algorithm for the evaluation of PI terms could be used in order to use different PI constants for charging ($V_{C_b} \leq 12$V) and discharging ($V_{C_b} \geq 12$V) stages. On this basis, a more aggressive charging is possible to be adopted since the important factors on this stage are a fast rise and settling time. On the other hand, for the discharging the voltage overshoot and stability are the defining factors of K_p and K_i. Thus by absolving the evaluation of the PI terms from the two stages more accurate and precise results could be derived.

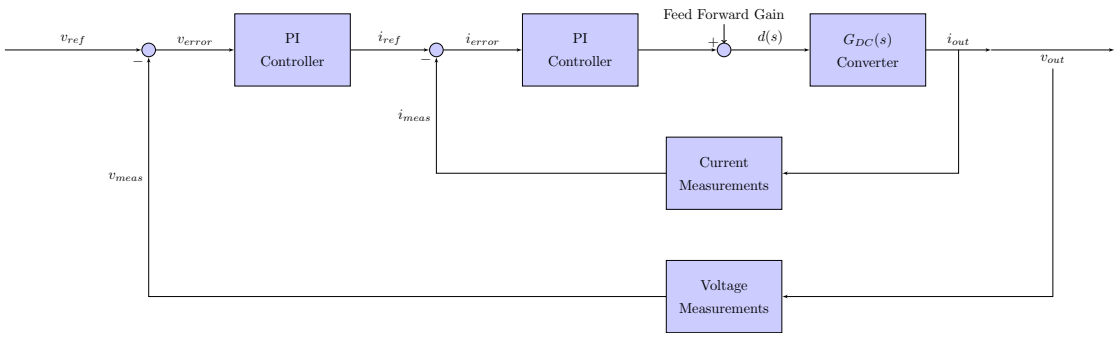


Figure 5.1: Cascaded Voltage-Current loop control.

In the future the storage unit should be tested also for the discharging stage. To achieve such operations some difficulties concerning the overcurrent protection of the DC-DC converter should

be overcome as well as programming optimization of the selected algorithm for integer numbers.

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