Assessment of the Reverse Operational Characteristics of SiC JFETs in a Diode-Less Inverter

G. Kampitsis, P. Stefas, N. Chrysogelos, S. Papathanassiou and S. Manias
Electric Machines and Power Electronics Laboratory
National Technical University of Athens
9 Iroon Polytehniou St., 15780 Zografos, Greece
Email: gkampit@central.ntua.gr

***Abstract*—In this paper, a thorough analysis of the reverse conduction characteristics of vertical trench (VT) Silicon Carbide (SiC) junction field effect transistors (JFETs) is performed. While these power devices do not encompass a body diode, traditionally present in conventional Silicon (Si) based semiconductors, such as the metal-oxide semiconductor field-effect transistors (MOSFETs), they exhibit notable reverse properties such that an external antiparallel diode can be considered redundant in most power converter applications. Both enhancement mode and depletion mode SiC JFETs are examined in terms of static reverse operation. Their performance is initially validated through simulation testing by constructing new SiC JFET models in Pspice model editor. The theoretical and simulation results are confirmed via experimental testing in a three phase voltage source inverter with and without antiparallel SiC diodes. When a gate drive that protects the semiconductor during reverse operation, while presenting great switching and forward conduction characteristics, is introduced, the power converter's overall performance is investigated paying particular attention to power losses during the dead time interval.**

Keywords — drive circuit; inverter; reverse operation; saturation; SiC JFETs

I. INTRODUCTION

Distinctive features of the next generation converters are their increased performance, high reliability and ability to operate under adverse climatic conditions such as high temperatures and severe radiation [1]-[3]. These requirements can only be met by replacing the conventional Si based semiconductors with more efficient and versatile power switches. Wide Band Gap (WBG) semiconductors exhibit favorable performance characteristics such as high blocking voltage capability, low on state resistance, low switching losses, high current ratings and high thermal conductivity [4]-[6]. Among them, Silicon Carbide (SiC) junction field effect transistors (JFETs) are considered to be the most technologically mature and structurally stable power devices, making them commercially available since 2008. Utilizing this viable technology in power converters is the enabling factor for increasing renewable energy sources (RES) penetration levels and developing electric vehicles (EV).

Most power converters require a diode connected antiparallel to each transistor in order to allow reverse power flow. Although vertical trench (VT) SiC JFETs do not have a body diode, they are bidirectional devices. Yet, the research attempts towards reverse operation of a SiC JFET are still limited, especially in power converters applications. More specifically, the ability of synchronous rectification is recorded in [7], indicating that under a certain current level, the reverse voltage drop of the enhancement mode (EM) JFETs can be lower than that of a diode rectifier, thus reducing the conduction loss. Authors of [8] mention the dependence of the voltage drop across the channel on the gate-to-source voltage during the cutoff state and they focus on the reverse recovery characteristics of the EM SiC JFETs. Yet, no mention has been made on the device's reverse current limits and its operational restrictions. An analysis of the reverse characteristics of depletion mode (DM) VT JFETs solely under gate-to-source short circuit conditions (i.e. during on-state) is found in [9], while, more recently, a comprehensive study of the reverse conduction properties of EM VT JFETs was realized in [10].

An RCD network connected to the output of a current amplifier IC is typically employed in order to drive efficiently the gate of the power switch [3], [10]-[12]. Moreover, a common strategy is to operate the semiconductor close to its breakdown voltage V_b. Adopting these driving techniques during reverse operation, not only do they introduce excessive power losses, but also may result in unpredictable conditions or even destruction of the power switch, due to great forward gate current, as will be explained later.

The aim of this paper is to perform a comparative study between the reverse conduction properties of normally-off (or EM) and normally-on (or DM) SiC JFETs. To this end, the design and implementation of a universal gate drive circuit for SiC JFETs that offers safe and efficient both reverse and forward operation, while exhibiting great switching performance, is an accessional objective of this paper. Once the reverse saturation curves of both SiC JFETs have been exported from experimental data, an estimation of the necessity of adding antiparallel diodes in a three phase voltage source (VS) inverter is made.

The paper is structured as follows: The principles of the reverse operation of both EM and DM SiC JFET are outlined in Section II and the proposed driving scheme is presented in Section III. An assessment of the performance of the diode-less three phase inverter topology under static and dynamic

This work has been supported by the project Anti-SiC (*09-SYN-32-1181, Program SYNERGASIA-2009, GSRT*).

conditions, is provided in Section IV. The main conclusions are summarized in Section V.

II. REVERSE CONDUCTION CHARACTERISTICS

The lateral channel (LC) JFET is a modern variant of SiC JFETs, the cross section of which is illustrated in Fig. 1(a). In the same figure its electrical equivalent circuit is also depicted. Being a normally-on device, a negative gate-to-source voltage, lower than the pinch-off voltage (V_p) is needed in order to turn it off. A typical range of V_p is between -16 V to -26 V. An important feature of this power device is the antiparallel body diode. However, the forward voltage drop of the body diode is relatively high compared to the on-state voltage drop of the channel at rated current densities [13]-[15] while the design of a commercial gate driver is revealed to be too challenging due to the variance of V_p [11].

Another commercially available SiC JFET is the vertical trench which can be either normally-on or normally-off, depending on the thickness of the channel and the doping levels of the structure. A cross section of this particular SiC JFET is illustrated in Fig. 1(b), in which the fundamental and parasitic components are also depicted. In static operation, the p-n junctions formed across gate-to-drain and gate-to-source have been replaced by diodes, while the channel of the JFET is substituted by a current source. The pinch-off voltage V_p for the DM VT JFET is approximately -5 V while for the EM VT JFET is about +1 V. As can be seen from Fig. 1(b), no p-n junction is formed across the source and drain terminals of a VT SiC JFET and thus, no intrinsic body diode is present [16].

The DM SiC JET used in this paper is SJDP120R085 exhibiting 1200V breakdown voltage, 27A continuous drain current at 25°C and 75 mΩ typical on state resistance. Also, SJEP120R100 which is an EM SiC JFET having 1200V breakdown voltage, 17A continuous drain current at 100°C and 80 mΩ typical on state resistance is also examined within this article. A SiC diode SDP30S120 was selected as the antiparallel diode in the three phase inverter featuring 1200 V_{dc} blocking voltage and 30 A continuous forward current. In order to extract the static characteristics of a VT SiC JFET, a simple gate drive circuit shown in Fig. 2 is considered, consisting of a current amplifier IC and a series resistor R_{fwd}.

Since the SiC JFET is a bilateral power switch and structurally a symmetrical semiconductor device, it can be assumed that in reverse conduction, the source current will follow saturation curves similar in shape to the forward conduction, depending on the voltage drop V_{SD} and the controlling voltage V_{GD}. More specifically, if the controlling voltage V_{GD} drops below the reverse threshold voltage V_{p_r}, a pinch-off region will be formed closer to the source terminal of the power switch, leading to the saturation of the channel current. The equations describing the drain current during reverse operation can be derived by modifying the known equations of the forward conduction. Equation (1) refers to the linear region while (2) to the saturation region. I_{SDD_r} is the reverse saturation current and λ_r is the channel-length modulation parameter and is equal to the slope of the current waveform at saturation.

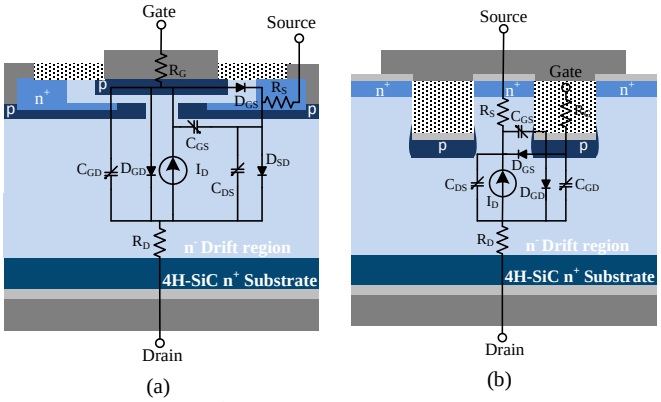

Fig. 1. Cross section of (a) a lateral channel and (b) a vertical trench SiC JFET with their equivalent electrical circuits.

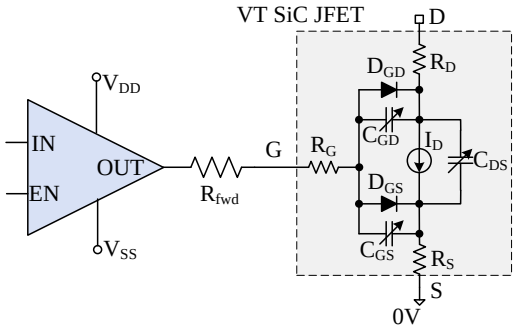

Fig. 2. Simple gate drive topology for extracting static characteristics of a VT SiC JFET.

$$I_D = I_{DSS\_r}\left[2\left(1-\frac{V_{GD}}{V_{p\_r}}\right)\left(\frac{V_{DS}}{V_{p\_r}}\right)-\left(\frac{V_{DS}}{V_{p\_r}}\right)^2\right] \quad (1)$$

$$I_D = I_{DSS\_r}\left(1-\lambda_r V_{DS}\right)\left(1-\frac{V_{GD}}{V_{p\_r}}\right)^2 \quad (2)$$

However, in all power electronics applications utilizing SiC JFETs, the controlling voltage is V_{GS} and consequently, V_{GD} is a dependent variable calculated using (3) as the difference between V_{GS} and V_{DS}.

$$V_{GD} = V_{GS} - V_{DS} \quad (3)$$

Under this constraint, and since a VT SiC JFET is at on-state when V_{GD} is greater than V_p, this power device may conduct reverse current when inequality (4) is met.

$$V_{DS} < V_{GS} - V_p \quad (4)$$

More specifically, imposing a negative voltage across V_{DS} reduces the width of the depletion region within the channel, allowing the current to flow backwards. Inequality (4) suggests that the minimum voltage drop across a SiC JFET during reverse conduction is closely associated to the instantaneous gate-to-source voltage applied. Another notable conclusion drawn from (4) is that during reverse operation, a DM SiC JFET, that has negative pinch-off voltage, exhibits lower power losses in comparison with an EM SiC JFET having positive V_p.

During reverse conduction, it is possible that the equivalent diode D_{GD} shown in Fig. 1(b) exceeds its threshold voltage V_{GD_th} and hence, a significantly high current is provided by the gate drive following a diode's *V-I* characteristic curve. Equation (5) specifies the drain-to-source voltage range in which this case appears.

$$V_{DS} < V_{GS} - V_{GD\_th} \tag{5}$$

Given that the gate drive circuit is capable of providing the required current, no saturation drain current will be observed as V_{GD} is higher than V_{GS} and the channel will never be pinched-off. However, the system reliability and integrity is compromised since a high gate current may destroy the power switch. This phenomenon is highly likely to occur with a typical RCD network, commonly utilized to drive SiC JFETs considering that $R_{fwd} = 0$. On the contrary, if a gate drive has $R_{fwd} \neq 0$ during conduction, the gate current will be limited, just as the forward bias of D_{GD}. Thus, given that a forward resistor is present, the reverse drain current follows a saturation curve, the limit of which is determined by R_{fwd}. The experimentally obtained V_{GD}-V_{DS} curves, which are similar for both EM and DM SiC JFETs, for various gate-to-source voltages and R_{fwd}=100 Ω are depicted in Fig. 3. It can be observed that regardless of the applied gate-to-source voltage, as V_{SD} increases, all curves reach a constant value which can be considered equal to the threshold voltage V_{GD_th}. The pair (V_{DS},V_{GD}) at the knee of each curve is also indicated in the same figure.

Once V_{DG} reaches its threshold voltage, V_{GS} begins to drop, following the reverse voltage V_{DS} as outlined by (6) and hence, a high negative voltage is indirectly applied to the equivalent diode D_{GS}.

$$V_{GS} = V_{DS} + V_{GD\_th} \tag{6}$$

As illustrated in Fig. 4, when V_{SD} is higher than the initial gate-to-source voltage subtracted by V_{GD_th}, V_{GS} exhibits a linear decay having approximately a unitary slope. Moreover, excessive decrease of V_{DS} may lead the diode D_{GS} into the breakdown region, resulting in high current through both D_{GS} and D_{GD}, that would ultimately damage the device.

A. Depletion Mode VT SiC JFETs

In Fig. 5, the experimentally obtained V_{DS}-I_D characteristics of the SJDP120R085 DM SiC JFET are depicted both for forward and reverse operation. In the first quadrant, V_{GS} is the controlling voltage varying from -5 V to +2 V whereas in the third quadrant, V_{GD} is the controlling voltage varying from -5 V to +2.95 V. The higher the V_{GD} bias, the greater the saturation level of the drain current since the conducting channel becomes wider. It can also be observed that, although the device is capable of handling high current densities during reverse operation, the reverse saturation current levels are much lower in comparison with the respective levels in forward conduction.

Applying a constant gate-to-source voltage while the drain current conduction is in reverse direction, the V-I

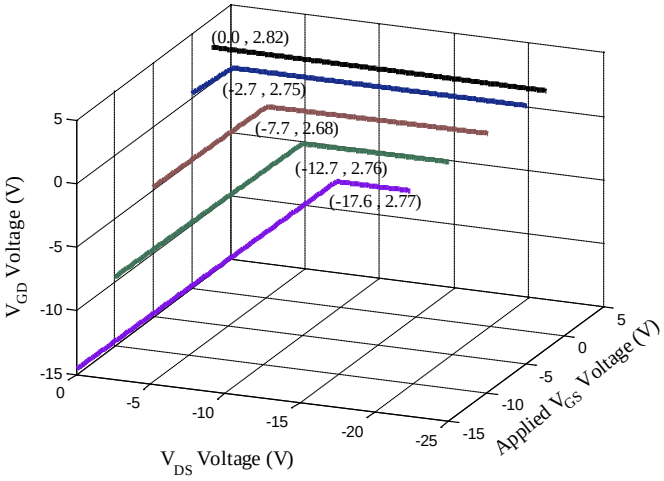

Fig. 3. V_{GD} voltage with respect to V_{DS} for various gate-to-source voltages and for R_{fwd}=100 Ω.

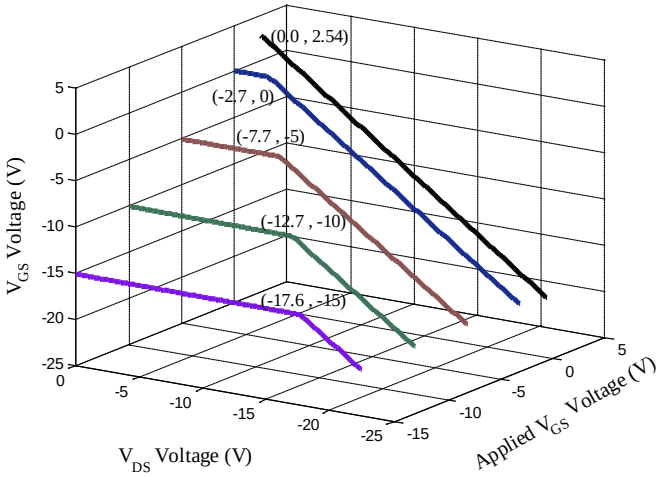

Fig. 4. V_{GS} voltage with respect to V_{DS} for various initial gate-to-source voltages and for R_{fwd}=100 Ω.

characteristics are extracted and are shown in Fig. 6. Each curve is substantially derived from successive shifting over the reverse characteristic curves of Fig. 5 as V_{GD} increases according to Fig. 3. Once D_{GD} reaches a constant voltage drop, depending on the gate current, the drain current saturates as in Fig. 5. Thus the saturation level depends only on the gate current and is the same for all V_{GS} controlling voltages. It can be noted that, for a given reverse drain current $I_{D,}$ the voltage drop across drain and source terminals depends on the applied voltage V_{GS}. The lower the voltage V_{GS} the more the depletion area extends into the channel, resulting to a greater conduction resistance. Thus, high conduction losses will be observed when the power device conducts reverse current during the cut-off state. Therefore, the controlling voltage V_{GS} applied from the driver circuit must be carefully chosen in order to minimize the reverse conduction losses. Furthermore, a VT SiC JFET should be prevented from operating close to the saturation current levels in order to avoid high gate current and restrain V_{GS} over the breakdown region.

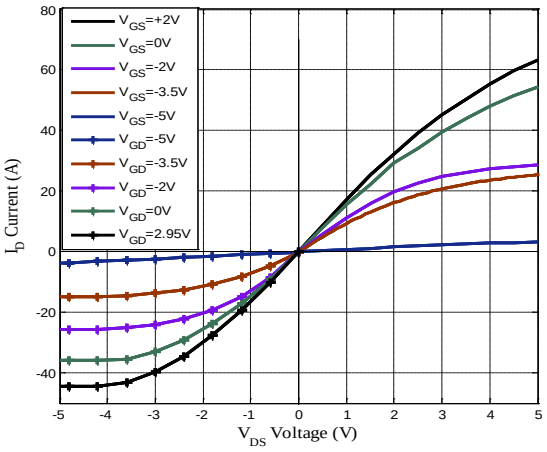

Fig. 5. V_{DS}-I_D characteristics of the SJDP120R085 during forward and reverse operation.

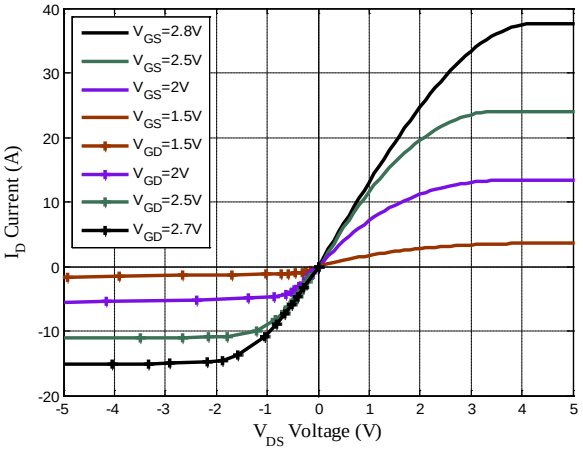

Fig. 7. V_{DS}-I_D characteristics of the SJEP120R100 during forward and reverse operation.

B. *Enhancement Mode VT SiC JFETs*

Following the same process as for the normally-on SiC JFET, the respective characteristic curves in the reverse conduction of the EM SJEP120R100 SiC JFET are presented in this section. In Fig. 7, the experimentally obtained V_{DS}-I_D characteristics in forward and reverse operation for various V_{GS} and V_{GD} voltages are illustrated. In comparison to the normal forward current conduction, the reverse saturation current levels are over 50% reduced.

In Fig. 8, the V_{DS}-I_D characteristics for reverse current conduction of the EM SiC JFET are presented, where V_{GS} is constant for each curve. As expected, the voltage drop across the EM SiC JFET during reverse conduction indicates dependence on voltage V_{GS} likewise the DM SiC JFET. Given that the threshold voltage V_p of an EM SiC JFET is positive and in accordance with (4), higher conduction losses will be recorded in comparison with a DM JFET, when applying the same V_{GS} voltage.

C. *Comparison*

Both devices are capable of conducting reverse current with insignificant power losses. During reverse operation, the DM JFET exhibits greater current ratings and lower power loss compared to the EM JFET. Since a VT SiC JFET should not operate under reverse saturation, the DM SiC JFET has wider safe operation margins for a given maximum output current of the gate drive.

In comparison with commonly used MOSFET semiconductors, SiC JFETs exhibit no reverse recovery current making them preferable commercial semiconductors. More specifically, MOSFETs have poor recovery characteristics of their body diode leading to large recovery time which may ultimately cause a short-circuit in a bridge leg configuration, when operating at high frequencies.

III. THREE PHASE INVERTER DESIGN

A. *Gate Drive Circuit*

In this section the requirements and limitations of efficiently driving a VT SiC JFET are discussed in order to maximize its performance. The ability of this JFET to conduct current in both directions makes the design of a gate driver

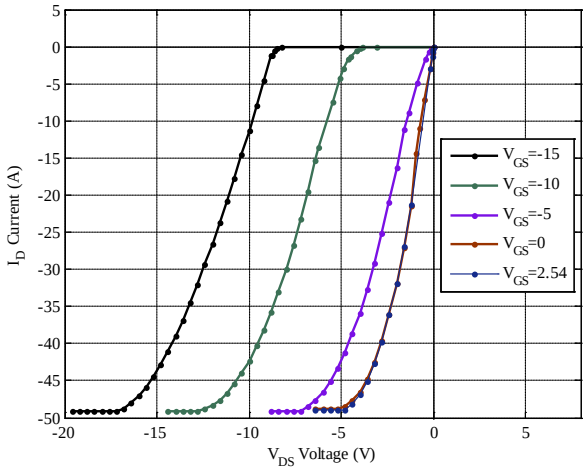

Fig. 6. V_{DS}-I_D characteristics of the SJDP120R085 at reverse operation when applying constant gate-to-source voltage.

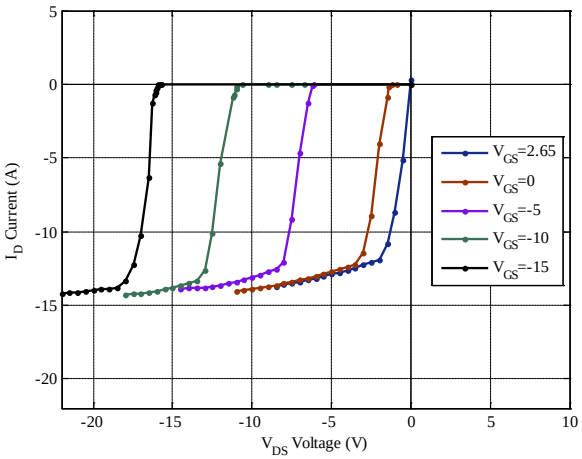

Fig. 8. V_{DS}-I_D characteristics of the SJEP120R100 at reverse operation when applying constant gate-to-source voltage.

even more challenging. An ac-coupled gate drive is utilized, the operational characteristics of which are described both in forward and reverse conduction [17]. The proposed gate drive schematic is presented in Fig. 9. The digital isolator ADUM2210 was selected to isolate the control signal, and IXDD_609 was used as the main current amplifier with a continuous current rate of 2 A. The power supply of the IC was set at V_{SS} = -15 V, and V_{DD} = +5 V, The output stage of the proposed drive is a modified RCD network consisting of three parallel branches and a ceramic capacitor C_g connected across the gate-source terminals.

Unlike a typical RCD driver that forces the SiC JFETs to operate close to their breakdown voltage, -15 V are applied through R_r and D_r yielding lower conduction losses in reverse operation. During the on-state, a positive voltage is applied to the gate through R_{fwd} and D_{fwd}. When forward biasing the equivalent diode D_{GS}, the depletion region in the channel is reduced and the saturation drain current increases (see Fig. 5 and Fig. 7). Respectively, the value of V_{GD} during reverse operation determines the negative saturation levels. Consequently, the performance of the driving circuit is largely dependent on the selection of the resistor R_{fwd}. In order to precisely determine the current provided by the gate drive, the V_G-I_G characteristics of both EM and DM SiC JFETs should be extracted. Fig. 10 depicts these characteristics for both equivalent diodes D_{GD} and D_{GS}. It can be observed that the threshold voltage of both diodes is 2.65 V at 25 mA for the EM and 2.7 V at 45mA for the DM SiC JFET. It should be noted that applying forward voltage greater than 3 V would result in excessive power losses at the gate drive while no improvement would be achieved in the semiconductor's performance.

At this particular application, the resistor R_{fwd} was selected to be 100 Ω, R_r=47 Ω while D_{fwd} and D_r are fast recovery Schottky diodes. The R_{ac}-C_{ac} branch is responsible for the transients with R_{ac}=5.1 Ω and C_{ac}=47 nF.

B. Simulation Results

An evaluation of the reverse conduction properties of the VT SiC JFETs in a three phase – two level VS inverter with and without antiparallel diodes is performed through simulation testing. New EM and DM SiC JFET models as well as the SiC diode SDP30S120 model were designed in Pspice model editor. The dc voltage was set at 400V while 10 A was selected as the peak load current. It should be noted that, in an inverter application, the two semiconductors of the same leg are ideally prevented from being in the conduction or the cutoff state simultaneously, regardless of the control strategy

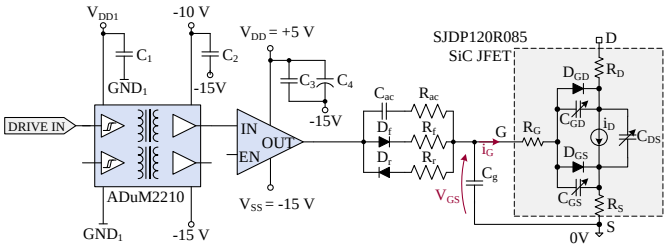

Fig. 9. Proposed gate drive circuit.

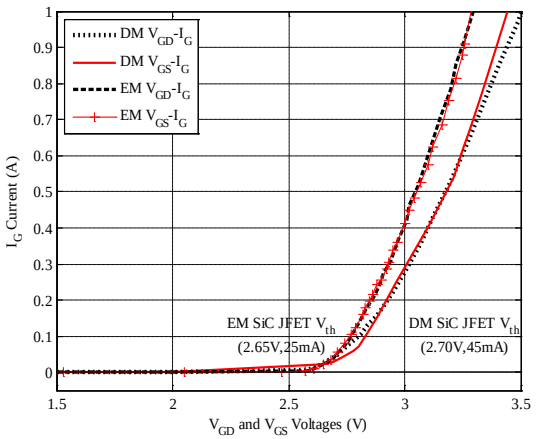

Fig. 10. V_{GS}-I_G and V_{GD}-I_G characteristics of the SJDP120R085 and SJEP120R100.

employed. However, in practice, a dead band T_{DB} is introduced at each transition phase, where both devices are off. Although the gate voltage of both semiconductors is -15 V during this interval and regarding an inductive load, the output current I_L may still conduct in reverse mode through one of the semiconductors of the same leg. A relatively large voltage drop will be observed at each transition in accordance with Fig. 6 and Fig. 8 and consequently, significant reverse conduction losses E_{rev} will be recorded according to (7). It should be noted that depending on the switching frequency and the dead band interval, the E_{rev} losses may be comparable to or even larger than the forward conduction losses.

$$E_{rev} = \int_0^{T_{DB}} V_{DS}(t) \cdot I_L(t)\, dt \qquad (7)$$

Here, a simple SPWM technique is adopted, having 1μs dead time. The dead time width has deliberately been oversized in order to highlight its impact on the system's efficiency. The simulation results describing the operation of the converter during reverse conduction are depicted in Fig. 11. The three waveforms within this figure illustrate the drain-to-source voltage drop of a single semiconductor when the inverter utilizes DM JFETs, EM JFETs or SiC JFETs with antiparallel SiC diodes. It is clear that the EM SiC JFET has the greatest negative voltage drop, thus exhibiting high power

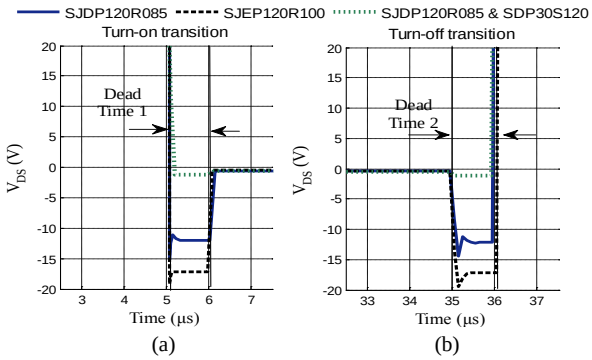

Fig. 11. Simulation results for the V_{DS} voltage drop during (a) turn-on and (b) turn-off of a single semiconductor in an inverter application utilizing DM SJDP120R085, EM SJEP120R100 and SiC JFETs with antiparallel SiC diode SDP30S120.

losses, while the antiparallel diode minimizes the reverse losses.

C. Experimental Validation

The theoretical and simulation results are validated through experimental testing in a three phase SiC-based VS inverter shown in Fig. 12. As expected, power losses are minimized by the addition of the antiparallel SiC diodes and are higher when utilizing normally-off SiC JFETs. This observation is indicated from the voltage drop at one semiconductor as depicted in Fig. 13 when utilizing different types of VT SiC JFETS and SiC diodes. Although the voltage difference is imperceptible, in forward conduction the EM SiC JFET exhibits the most favorable performance characteristics. The experimental results are consistent with the simulation results earlier presented (Fig. 11).

IV. Conclusion

In this paper, the potential of omitting the antiparallel diode in a VS inverter utilizing VT SiC JFETs is thoroughly examined. The reverse characteristics of both EM and DM SiC JFETs are experimentally derived indicating that they are bidirectional semiconductors exhibiting remarkably low reverse voltage drop when the controlling voltage V_{GS} is greater than the pinch-off voltage. In cases where $V_{GS}<V_p$, a relatively high voltage drop is recorded especially in a EM SiC JFET due to its positive threshold voltage. Although theoretically the reverse drain current can increase until reaching the structural limits of the channel, in practice, a saturation level is observed due to the limited supplied current of a typical gate drive. A gate drive circuit that exploits the device's forward conduction and switching characteristics while protecting it during reverse operation is proposed. After simulation testing and experimental validation it can be concluded that in a three phase VS inverter, the antiparallel diodes can be considered redundant as long as the dead band is kept small.

Fig. 12. Three phase VS inverter utilizing DM SJDP120R085 SiC JFETs.

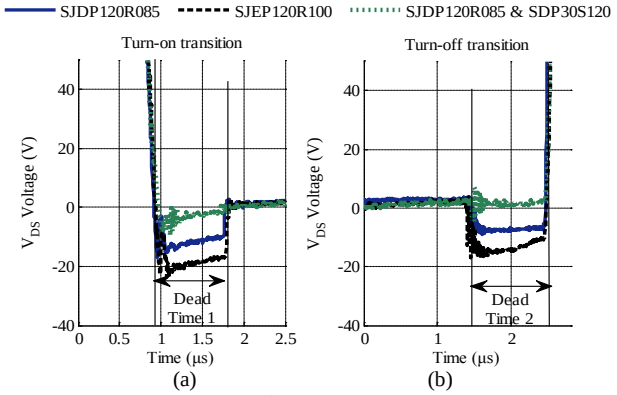

Fig. 13. Experimental results for the V_{DS} voltage drop during (a) turn-on and (b) turn-off of a single semiconductor in an inverter application utilizing DM SJDP120R085, EM SJEP120R100 and SiC JFETs with antiparallel SiC diode SDP30S120.

References

[1] C. Cass, R. Burgos, F. Wang, and D. Boroyevich, "Three-phase ac buck rectifier using normally-on SiC JFETs at 150 kHz switching frequency", in IEEE PESC, 2007, pp. 2162–2167.

[2] J. Biela, M. Schweizer, S. Waffler, J.W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors",in IEEE Transactions on Industrial Electronics, Vol 58 no 7, pp. 2872-2882, July 2011.

[3] J. Rabkowski, D. Peftitsis, H.-P. Nee, "Design steps towards a 40-kVA SiC inverter with an efficiency exceeding 99.5%" in IEEE APEC, 2012, pp. 1536-1543.

[4] A.M. Abou-Alfotouh, Inc.Empirion, NJ Bridgewater, "Comparison among SiC JFETs at 1 MHz hard-switched DC/DC converter", in IEEE IECON, Radun, A.V., 2005.

[5] Yutian Cui, M.S. Chinthavali, Xu Fan, L.M. Tolbert, "Characterization and modeling of silicon carbide power devices and paralleling operation", in IEEE ISIE, 2012, pp. 228–233.

[6] S. Waffler, S.D. Round and J.W. Kolar, "High temperature (>200◦C) isolated gate drive topologies for Silicon Carbide (SiC) JFET", in IEEE IECON, 2008, pp. 2867–2872.

[7] Lai, J.-S., Yu, H., Zhang, J., Alexandrov, P., Li, Y.; Zhao, J.H., Sheng, K., Hefner, A., "Characterization of normally-off SiC vertical JFET devices and inverter circuits", in IEEE IAS, 2005, pp. 404-409.

[8] Shillington R., Gaynor P., Harrison M., Heffernan B., "Applications of silicon carbide JFETs in power converters", in IEEE AUPEC, 5-8 Dec. 2010, pp. 1-6.

[9] Sheridan D. C., Chatty K., Bondarenko V., Casady J. B., "Reverse conduction properties of vertical SiC trench JFETs", in IEEE ISPSD, 3-7 June 2012, pp. 385-388.

[10] Cai, C., Zhou, W., Sheng, K., "Characteristics and application of normally-off SiC-JFETs in converters without antiparallel diodes" in IEEE Transactions on Power Electronics, 2013, pp. 4850-4860.

[11] S. Round, M. Heldwein, J. Kolar, I. Hofsajer and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter", in IEEE IAS, 2005, pp. 410–413.

[12] R. Burgos, Zheng Chen, D. Boroyevich, F. Wang, "Design considerations of a fast 0-Ω gate-drive circuit for 1.2 kV SiC JFET devices in phase-leg configuration", in IEEE ECCE, 2009, pp 2293–2300.

[13] P. Friedrichs and R. Rupp, ''Silicon carbide power devices-Current developments and potential applications,'' in IEEE EPE, 2005, pp. 1–11.

[14] B. Ållebrand and H.-P. Nee, ''On the choice of blanking times at turn-on and turn-off for the diode-less SiC JFET inverter bridge,'' in IEEE EPE, Aug. 2001, pp. 1–9.

[15] J. Rabkowski, D. Peftitsis, and H.-P. Nee "Silicon carbide power transistors: a new era in power electronics is initiated", June 2012, IEEE Industrial Electronics Magazine, pp. 17–26.

[16] "Silicon carbide enhancement-mode junction field effect transistor and recommendations for use", Application Note AN-SS1, SemiSouth Laboratories Inc.

[17] G. Kampitsis, S. Papathanassiou and S. Manias, "Performance consideration of an AC coupled gate drive circuit with forward bias for normally-on SiC JFETs", in IEEE ECCE, 2013, in press.